JVC

VIDEO TECHNICAL GUIDE

VIDEO CASSETTE RECORDER

BR-S422U

SA-R200U
TIME CODE GENERATOR

S-VHS Hi-Fi

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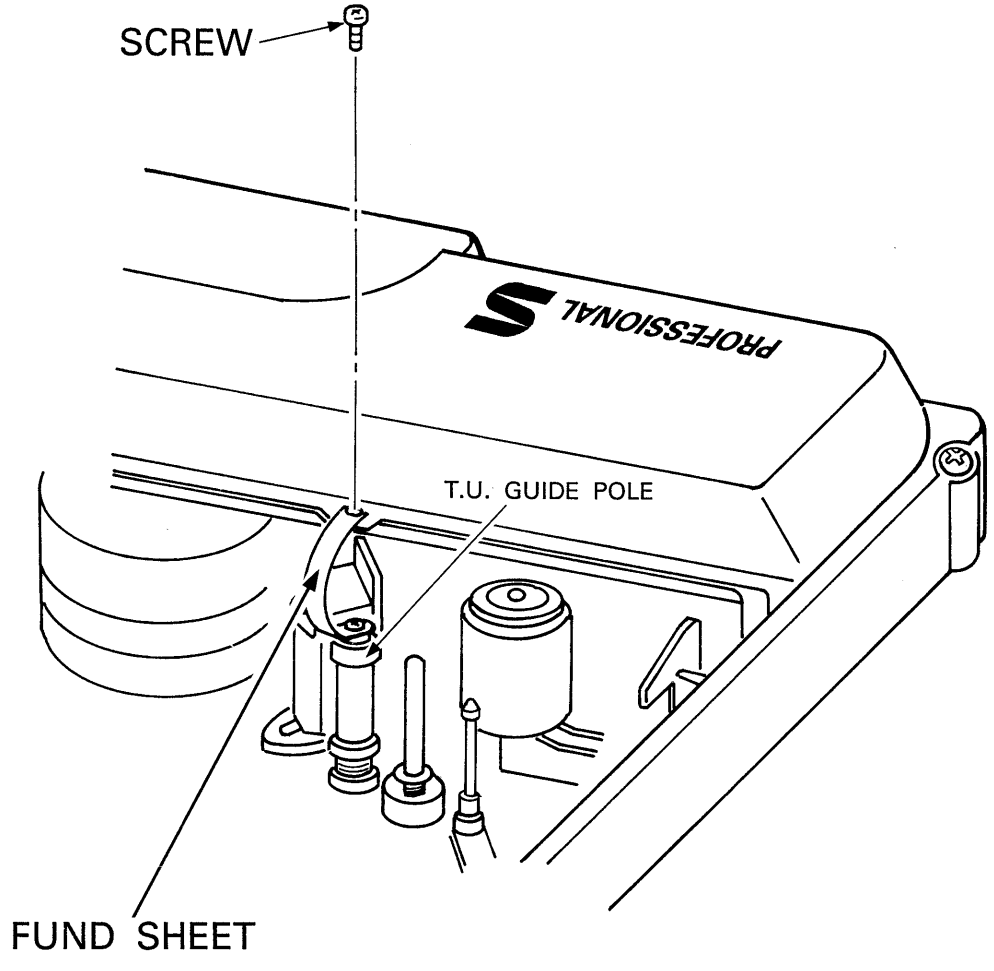
WARNING

• NOTE ON THE FUND SHEET

This VTR is additionally equipped with the fund sheet, which is installed between the upper part of the take-up guide pole and the left side cover in order to prevent the cassette tape from coming off the normal loading position (between the take-up guide pole and the capstan) and from being abnormally loaded outside the take-up pole when the cassette is inserted for loading.

For removing the left side cover, therefore, first remove the screw retaining the fund sheet to the left side cover. Moreover, when reassembling the side cover and the fund sheet, make sure to fix the fund sheet tightly to the side cover, otherwise it may cause tape damage, etc.



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SECTION 1
GENERAL DESCRIPTION

1.1 MAIN FEATURES

- Conforming to the epoch-making S-VHS format (more than 400 TV lines in horizontal resolution), the BR-S422 is capable of recording minute pictures. Moreover, the design policy pursuing the basic performance in the standard mode remarkably improves picture quality on the whole.
- The rotary head for Hi-Fi audio records and plays back superb Hi-Fi sound particularly excellent in frequency response, dynamic range, wow and flutter. Besides the Hi-Fi audio, the two-channel normal audio system with Dolby* noise reduction system also offers wonderful sound.
- High quality audio with the XLR audio input terminal that is reliable and advantageous for noise reduction.
- Compactness and light weight design for direct docking with a video camera (JVC KY-17B, KY-27 and KY-35). Systematization of the VTR and the dockable CCD video camera realizes resultful footworks.
- Aluminum die-cast body increases durability, rigidity and reliability of the VTR.
- Indication display with back light for easiness to see in dark places integrally shows lap time/tape counting, tape remainder in recording, audio level, operable battery time, hour meter, various warning.
- Smooth editing with the flying erase head and the new AEF system.
- Auto review function convenient for recording check.
- Insert recording available for recording audio and video on used cassette tapes.
- Built-in ear-speaker easy to check sound.
- Time code is recordable with optional time code generator.
- Low power consumption.

1.2 DIFFERENCE BETWEEN BR-S411 AND BR-S422

Item		BR-S411B	BR-S422
• General			
Format		VHS/S-VHS standard	←
Signal system		NTSC TV system	←
Tape speed		33.35 mm/sec	←
REC/PB time		120 minutes (with T-120 tape)	←
FF/REW time		Within 4 minutes (with T-120 tape)	Within 4 min 30 sec (with T-120 tape)
Power requirement		12 V DC	←
Power consumption		16 W	13 W
Power supply to camera		24 W max.	←
Dimensions		297(W) × 240(H) × 137(D) mm	287.5(W) × 244(H)* × 131.5(D) mm * Main unit: 214.5(H) mm (Except battery)
Weight : Main unit		4.0 kg	3.2 kg
With Battery and Tape		4.9 kg	4.2 kg
• Video section			
Y/C input (50-pin connector)		Y : 1.0 Vp-p, 1 kΩ, unbalanced C : 0.286 Vp-p, 1 kΩ, unbalanced (Burst)	←
Video output (BNC connector)		1.0 Vp-p, 75 Ω, unbalanced	←
Y/C output (7-pin connector)		Y : 1.0 Vp-p, 75 Ω, unbalanced C : 0.286 Vp-p, 75 Ω, unbalanced (Burst)	←
Horizontal resolution (color)	S-VHS	More than 400 TV lines	←
	VHS	More than 240 TV lines	←
Video S/N ratio (color)	S-VHS	46 dB (Rhodeschwarz measurement)	←
	VHS	45 dB (Rhodeschwarz measurement)	←
• Audio section			
Track		4 tracks (Hi-Fi: 2, Normal: 2)	←
LINE input		–20/+4 dB, 10 kΩ, balanced –60 dB, 3 kΩ, balanced	← (–20 dB: 50-pin connector)
LINE output		–6/–20 dB, 600 Ω, balanced	–6 dB, 1 kΩ, unbalanced
Earphone output (ø 3.5 mm mini jack)		–25 to –45 dBs, 8 Ω	–60 to –12 dBs, 8 Ω
• Hi-Fi audio			
Frequency response		20 Hz to 20 kHz	←
Dynamic range		More than 80 dB	←
Wow and flutter		Less than 0.007 % (WRMS)	←
• Normal audio			
Frequency response		40 Hz to 12 kHz	50 Hz to 12 kHz
Audio S/N ratio		More than 48 dB (NR Switch ON) More than 44 dB (NR Switch OFF) Distortion rate : 3 %	←
Wow and flutter		Less than 0.25 % (WRMS)	Less than 0.15 % (WRMS)
• Others			
Auto cleaning		×	○
Hour meter		×	○ (digital)
OPERATE-ON		Switch	Operation cover
Time code		Optional (external)	Optional (built-in possible)
Battery pack		NB-G1	NB-G1, NP-1
AUTO REVIEW		×	○
Tape remainder indication		×	○
Built-in speaker		×	○
REC Tally lamp		×	○

SECTION 2
POWER SUPPLY CIRCUIT

2.1 SUPPLY POWERS

Power supplied to the set through the DC IN or the BATT IN terminal is selected by RY1 of the POWER CTL board and then supplied to the REGULATOR board via the main switch and the breaker.
In the REGULATOR board, the supply voltage is transformed to the specific voltages for the AL and SW systems.
The AL voltages are turned on when the main switch of the VTR is on and it is supplied to the syscon, the display microcomputer, etc.
The SW voltage is controlled by the syscon and it is converted into SW 12 V, SW 9 V and SW 5 V powers. SW 5 V and SW 9 V are generated by the switching regulator, and their voltages are controlled by changing the phase of the sawtooth waveform output from IC1 and they are switched by Q3, Q4 and Q5.
SAVE 9 V is used when this set is used as the VTR of the GY-X2 video camera. In concrete, when the GY-X2 docked with this VTR is in the POWER SAVE mode and the VTR is turned off, SAVE 9 V is used to output the camera's video and audio signals through the VTR OUT terminal. For a reference the BR-S422 is incapable of outputting those signals alone in the POWER SAVE mode since the power functions as same as for the SW system in that event.

● Operational status of VTR and video camera which are docked as one set

Note: When the BR-S422 and GY-X2 video camera are docked with each other, power on/off status of respective units is different from each other in the POWER SAVE mode.

Camera's OPERATE switch setting	Camera's power status	Power supply to BR-S422	VTR of GY-X2
ON	ON	ON	ON
SAVE	ON	OFF	ON (EE only)
OFF	OFF	OFF	OFF

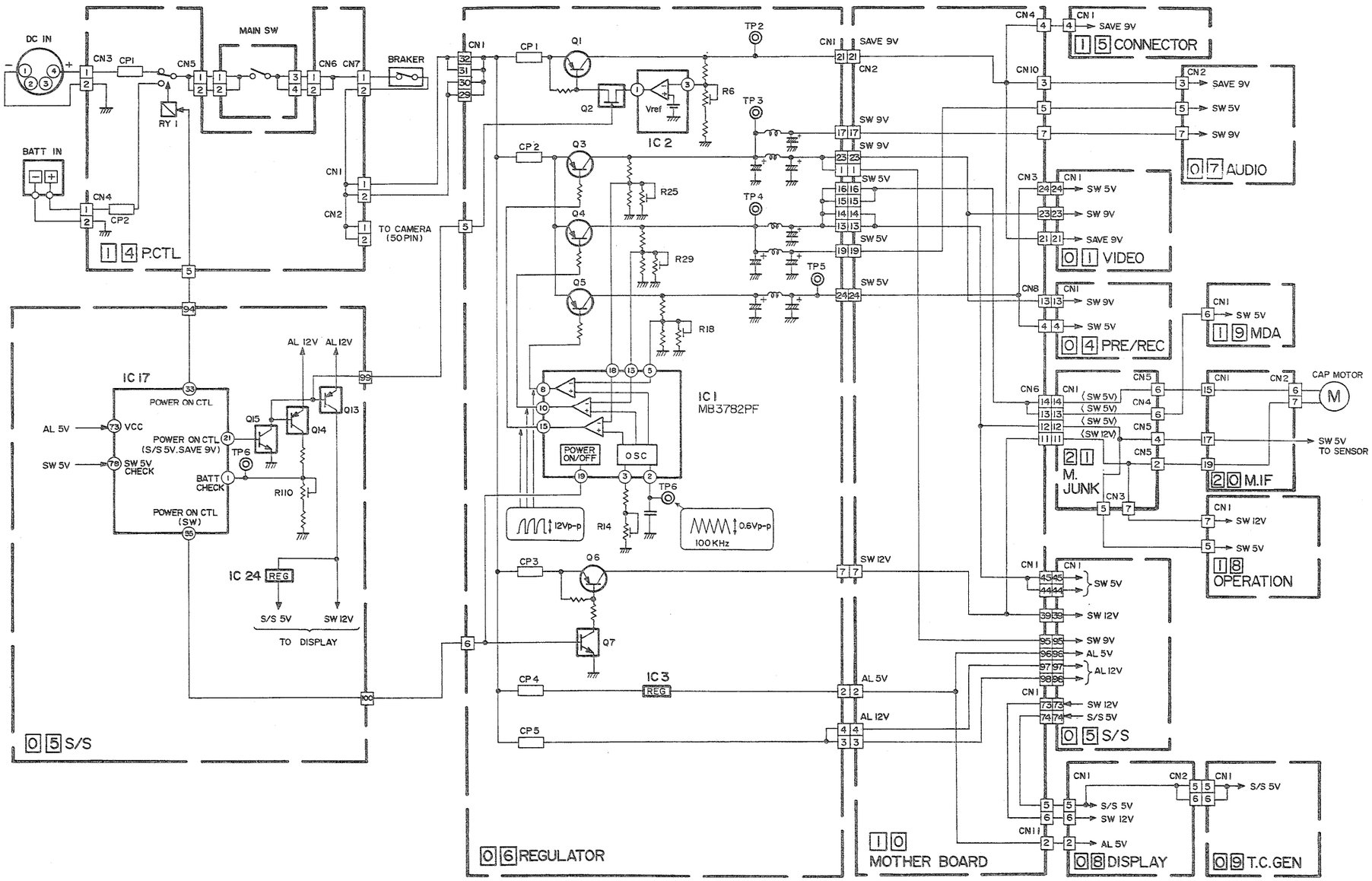


Fig. 2-1-1 Power supply circuit

2.2 POWER CONTROL

IC17 of the S/S board is the main microprocessor which is operated with AL5V power.
This microprocessor controls power supply as follows.

Pin No.	Name	Description
1	BATT	To check supply voltage. Enters the set in the BATT WARNING mode with voltage down by 10.95 V DC.
21	POWER ON CTL (SAVE)	To control S/S 5 V, SW 12 V (both generated in the S/S board) and SAVE 9 V powers. S/S 5 V is supplied to the DISPLAY board and the TC board, SW 12 V is used for the LED and back light of the DISPLAY board.
33	POWER ON CTL	To output RELAY CONTROL pulse to the POWER CTL board.
55	POWER ON CTL (SW)	To control SW 9 V, SW 5 V and SW 12 V generated by the REGULATOR board.
73	Vcc	AL 5 V input as the source power of the microprocessor.
78	SW5V CHECK	To check supply condition of SW 5 V power. When this power is not supplied, the mechanism is off operation since it operates with the SW 5 V power.

Table 2-2-1

2.3 OPERATION OF POWER CTL BOARD

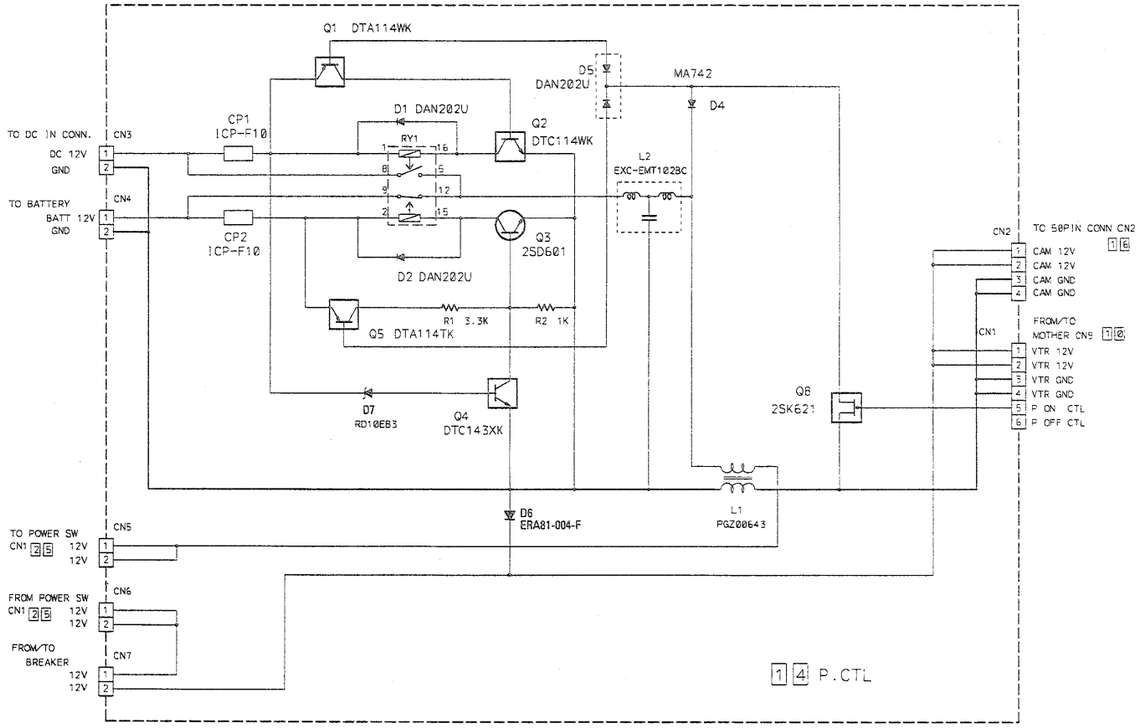


Fig. 2-3-1 POWER CTL board

The POWER CTL board switches between power inputs from the DC IN and BATT IN connectors.
In the BR-S411 power input is switched by the diode, however, it has the following disadvantages.

1) High rate of power consumption (1 W approx. because of voltage loss made by the diode).
2) Earlier low battery indication than its real life due to the voltage drop by a diode.

The BR-S422 improves those disadvantages by incorporating the latching type relay for switching power supply. This switching system maintains the switching mode that was once set by current flow in the internal coil of the relay without further current flow.

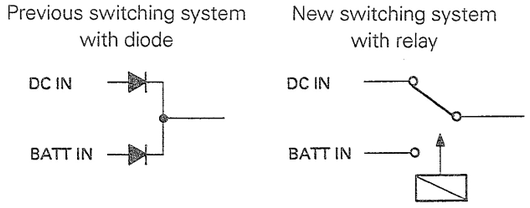


Fig. 2-3-2

The switching operation of the relay system will be described below. First, RY1 has two switches which are alternately turned on and off to switch the power supply without fail.
When power is supplied through the DC IN, the emitter and the base of the digital transistor Q1 are supplied with 12 V power. However, the base current flows through D5 and D4 to respective circuits (mainly to capacitors) of the VTR section. Therefore, the potential of the base does not turn to H level immediately after the power supply, but it has L level for a moment when current flows to capacitors of respective circuits, and Q1 is turned on in this short period. Consequently, Q2 is turned on and current flows through the coil of the relay to switch the power line to the DC IN.
On the other hand, voltage supplied from the DC IN flows via D7 to Q4 to turn it on while Q3 is accordingly turned off to prohibit operation of the switch for the BATT IN side. Q4 is a transistor to give priority to the DC IN line.
Secondly, when power is supplied through the BATT IN, Q4 does not turn on while Q5 and Q3 are turned on to switch the relay to the BATT IN side.
When the whole circuits of the VTR are on, the syscon supplies POWER ON CTL pulse to Q1 and Q5 via the pin ⑤ of CN1. This operation, which is provided on the assumption that the relay switch may fall in poor contact if a strong shock is given to the VTR, supplies current to the internal coil of the relay every two seconds to avoid abnormal switching of the relay if such a trouble occurs. However, the relay is highly reliable to shock and any abnormal switching owing to poor contact cannot be expected in usual use.

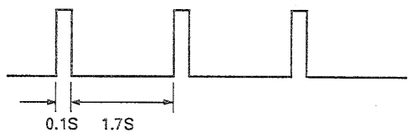


Fig. 2-3-3 Power ON CTL

The following explains about the case that power is supplied to the DC IN during active power supply from the BATT IN. In that event, Q4 is turned on while Q3 is turned off, however, the relay is maintained in the BATT IN side and it will be switched to the DC IN side only when the POWER ON CTL pulse is supplied to the base of Q1. In another case that power is supplied both to the DC IN and BATT IN, disconnection of the DC IN turns off Q4 and D4's cathode voltage drops down to 0 V. However, this voltage drop is not figured in a straight line but in a slow curve to 0 V. The beginning of voltage drop is detected by the base of Q5 together with functions of D4 and D5 and Q5 momentarily turns on to switch the relay to the BATT IN side.

2-2

SECTION 3
SYSCON/SERVO CIRCUIT

3.1 SYSTEM CONTROL SECTION

3.1.1 General

This model has two CPUs in the syscon circuit of the S/S board and the DISPLAY board (IC17 in the former and IC1 in the latter). Their controls of respective boards are serially operated in consideration of the expansibility and reduction of wires.

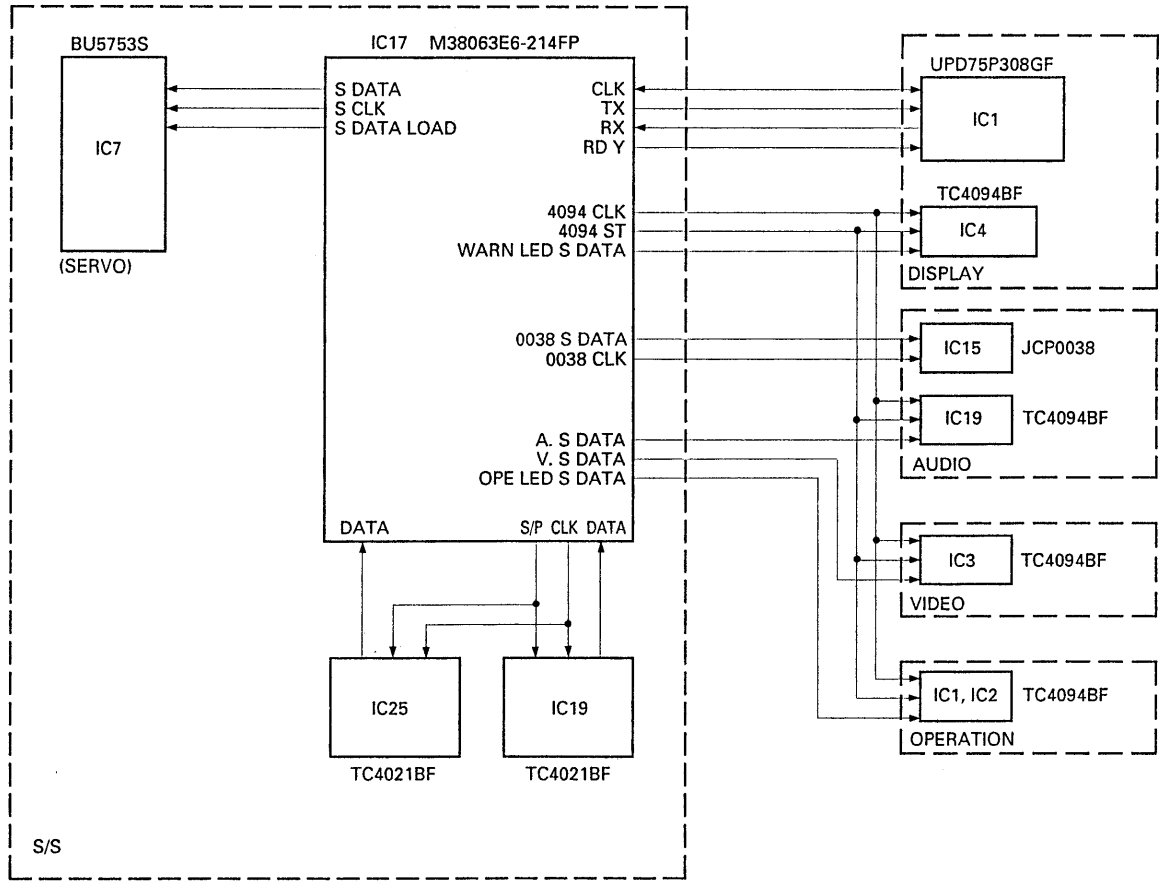


Fig. 3-1-1

3.1.2 Syscon CPU

IC17 is an 8-bit single chip microcomputer, which manages and controls VTR mode by means of its output ports.
IC1 on the DISPLAY board is a 4-bit single chip microcomputer, which controls time codes for the display indications by transmitting and receiving signals to/from the syscon CPU synchronizing with the clock.
Transmission and reception timing is shown in Fig. 3-1-2 while pin functions of the syscon CPU are shown in Table 3-1-1.

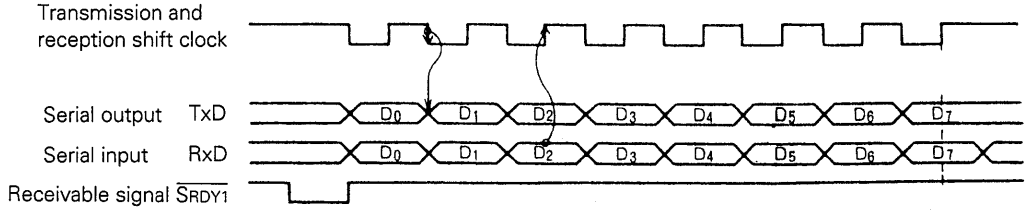


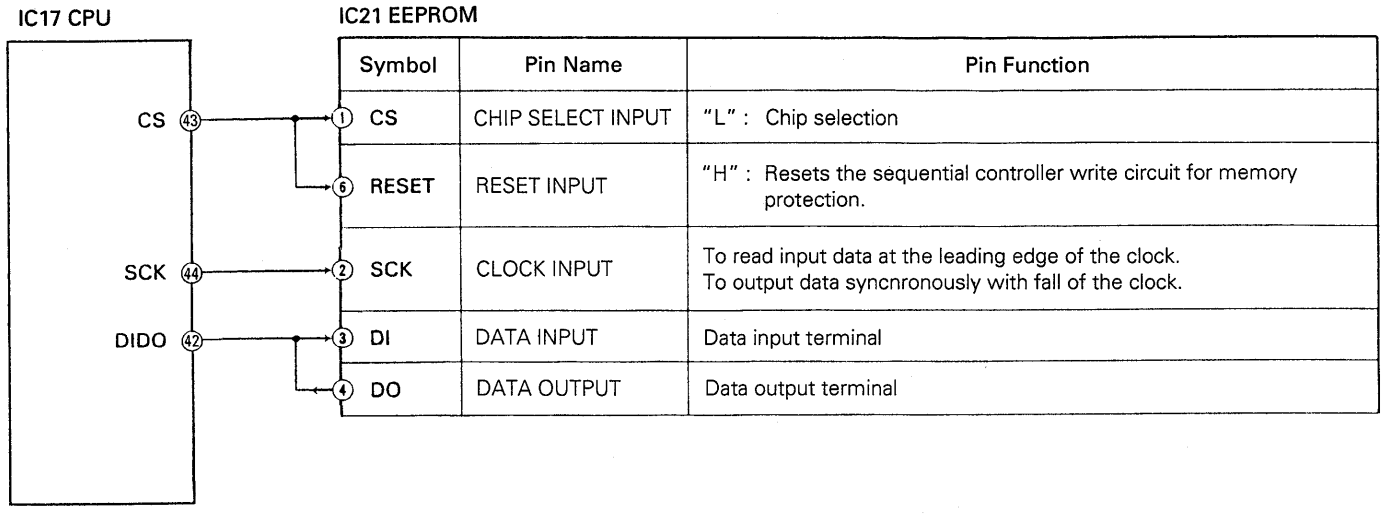
Fig. 3-1-2 Serial transmission and reception timing

● Syscon CPU pin functions

Pin No.	IN/OUT	NAME	DESCRIPTION
1	IN	B	Detection of remaining batery-operated time. BATT WARNING at 10.95 V DC.
2	IN	2.5/5V	Not used in BR-S422 Discrimination between STBY and SAVE1 modes of GY-X2 camera
3	IN	CAM ON/STBY	Not used
4	IN	END SENSOR	End sensor input detected : H
5	IN	START SENSOR	Start sensor input detected : H
6	IN	TU REEL FG	TU REEL FG input
7	IN	SUP REEL FG	SUP REEL FG input
8	IN	LCD RDY	For module communication control of display Microprocessor requests data to display : H
9		LCD CLK	CLOCK
10	IN	LCD TX	TRANS – On detecting L level of RDY signal, S/S transmits/receives
11	OUT	LCD RX	RECEIVE data to/from display synchronizing with CLK pulse.
12		SW POINT	Not used
13	OUT	CAP DRV	For driving capstan motor. In modes without servo : DC voltage output (FF, REW)
14	OUT	A TONE	ALARM TONE pulse output
15	IN	CAP FG	CAPSTAN FG input
16		CFP IN	Not used
17	IN	OPE COVER OPEN	Detection of operation cover status. Open : H
18	IN	CAMERA ON	Detection of camera ON/OFF status. ON : L
19	IN	F. SERVO CTL	In REC only. When FRAME SERVO is well-timed : H
20		(Prohibited)	
21	OUT	POWER ON CTL	For display. Control of S/S 5 V and SW 12 V powers.
22	OUT	VTR STATUS	VTR STATUS data output to camera
23	IN	CAMERA COM	Not used. Serial command from camera in GY-X2.
24	IN	PB CTL	PB CTL pulse input
25	IN	DFF	DRUM FF input
26		CNV	GND
27	IN	RESET	RESET input for microprocessor
28		REC OUT	Not used
29	OUT	FULL-E	Full erase ON/OFF control
30		X IN	4.9 MHz oscillation block
31		X OUT	
32		Vss	GND
33	OUT	POWER ON CTL	For control of relay of POWER CTL board. Constant pulse output.
34		POWER OFF CTL	Not used
35	OUT	OPE LED S DATA	Serial data output for operation LED
36	OUT	WARN LED S DATA	Serial data output for warning LED
37	IN	DATA IN	Serial data input from TC4021 (IC25)
38	OUT	4021 CLK	CLOCK output to control TC4021 (IC19, IC25)
39	OUT	4021 S/P	Control signal output for TC4021 (IC19, IC25)
40	IN	DATA IN	Serial data input from TC4021 (IC19)
41	IN	JIG	Input port for FULL REPEAT RUNNING mode. Grounding TP7 enters the set in the RUNNING mode.
42	IN/OUT	D I/O	Data input/output
43	OUT	CS	CHIP SELECT output – for EEP ROM control
44	OUT	EEP CLK	CLOCK output
45	OUT	MOTOR CTL	For control of mode motor (REV)
46	OUT	MOTOR CTL	For control of mode motor (FWD)
47	OUT	0038 CLK	CLOCK OUTPUT for control of JCP0038 (IC15) of AUDIO board
48	OUT	0038 S DATA	DATA OUTPUT for control of JCP0038 (IC15) of AUDIO board
49	OUT	4094 STB	Control signal output for output booster ICs (TC4094) of AUDIO,
50	OUT	4094 CLK	VIDEO, DISPLAY, OPERATION boards

Pin No.	IN/OUT	NAME	DESCRIPTION
51	OUT	VIDEO REC	VIDEO CTL signal. In REC mode : H
52	OUT	VIDEO PB	" In PB mode : H
53	OUT	V. REC MUTE	" In REC mode : L
54	OUT	VIDEO S DATA	Serial data output for control of IC (TC4094) of VIDEO board
55	OUT	POWER ON CTL	Power ON/OFF control for SW system
56	OUT	STOP CTL	Control of REC WARNING signal to be sent to camera section
57	OUT	EE (H)	In EE picture output : H
58	OUT	REC WARN	Control of "REC WARNING" (pin 49) of 50-pin output In REC mode : 5 V, In REC PAUSE mode : 2.5 V, In other modes : 0 V 5 V and 2.5 V pulses output when warning happens in REC mode.
59	OUT	BATT WARN	Pulse output in WARNING mode
60	OUT	FLY ON	Flying Erase head control
61	OUT	YNR	Pulse output synchronizing with D. FF in PB mode
62	OUT	ZFE CTL	Control of Zero Frame Editing
63	OUT	A S DATA	Serial data output to control TC4094 of AUDIO board
64	OUT	A REC MUTE	FM audio control signal. In REC mode : L
65	OUT	CAP REV	Capstan rotation direction indication. In REV mode : H
66	OUT	DRUM ON	Drum rotation control
67	OUT	S DATA	Serial data output to control IC (BU5735S) of SERVO board
68	OUT	SERVO DATA LOAD	Control signal output for IC (BU5735S) of SERVO board
69	OUT	PB CTL DUTY	Control of VISS write-in. In Writing : H
70	OUT	S CLK	Serial clock output to control IC (BU5735S) of SERVO board
71	OUT	S MODE	Seervo ON/OFF output. When Servo ON : L
72	OUT	CAP POWER UP	When capstan gain goes up : H
73	IN	Vcc	+5 V DC
74	IN	VREF	A/D converter power supply
75		AVss	GND
76	IN	AUDIO R	Signal input for audio level meter (R-ch)
77	IN	AUDIO L	Signal input for audio level meter (L-ch)
78	IN	SW 5 V CK	For SW 5 V check
79	IN	KEY B	Operation key input port. REC/INSERT
80	IN	KEY A	Operation key input port. STOP, REW, FF, PLAY, STILL, EJECT.

3.1.3 EEPROM (M6M80011AP)



Symbol	Pin Name	Pin Function
① CS	CHIP SELECT INPUT	"L" : Chip selection
⑥ RESET	RESET INPUT	"H" : Resets the sequential controller write circuit for memory protection.
② SCK	CLOCK INPUT	To read input data at the leading edge of the clock. To output data syncnronously with fall of the clock.
③ DI	DATA INPUT	Data input terminal
④ DO	DATA OUTPUT	Data output terminal

Fig. 3-1-3 IC21 pin functions

- **Outline of IC21 functions**

IC21 is a 1024-bit (16 bits × 64 words) CMOS EEPROM (Electrically Erasable and Programmable ROM) which is capable of electrically writing and erasing data.

This IC which is a clock synchronous serial input and output type records total operation hours of the drum rotation and reads in data at the leading edge of the clock and outputs data synchronously with the fall of the clock.

Each data is divided at a unit of 8 bits, and the first 8-bits unit is used for mode, the second 8-bits is for address and the rest composed of 16 bits is input or output data. The mode can be specified in five ways of WRITE, READ, WRITE ENABLE, WRITE INHIBIT, and STATUS OUTPUT.

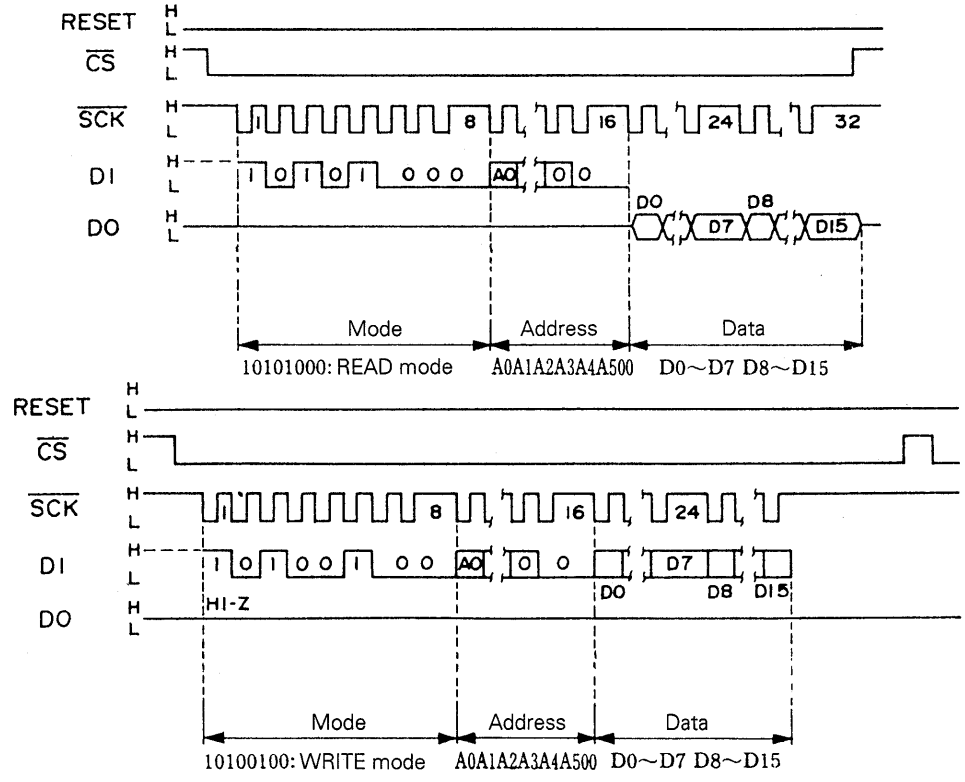


Fig. 3-1-4 READ and WRITE modes timing charts

3.1.4 DIP switch on DISPLAY board

Initial setting	Function	Remark
SW3-1 : OFF -2 : OFF -3 : OFF -4 : OFF -5 : OFF -6 : OFF -7 : OFF -8 : OFF	SW3-1 : BM switch ON : LTC's bi-phase mark phase correction circuit is activated. OFF: LTC's bi-phase mark phase correction circuit is inactivated.	On/off setting of the bi-phase correction bit of the 27th bit of the LTC code format.
	SW3-2 : Not used	
	SW3-3 : AEF switch (having priority over others) OFF: Normal operation (by AEF switch on the side panel) ON : AEF is inactivated (without back-space and picture dropout).	
	SW3-4 : EEP ROM CLEAR switch OFF: EEP ROM CLEAR circuit is inactivated. ON : EEP ROM CLEAR circuit is activated.	Adds up operation hours of drum rotation. With this switch set to ON, the EEP ROM can be cleared by depressing the REC button and SELECT button simultaneously for more than 3 seconds. After clearing, make sure to reset this switch to OFF position.
	SW3-5 : ZEF (Zero Frame Editing) switch OFF: Normal operation ON : Zero frame editing is inactivated. (Recording slightly overlaps at editing point at which time code is partially erased.)	Effective when the AEF switch is set to OFF.
	SW3-6 : DEW switch OFF: Normal operation ON : Dew warning is forcibly cancelled and recording is enabled. (Dew warning appears in the display.) Monitor speaker's alarm sound is cut off.	This switch is used for cancelling dew warning mode for forcible recording. This should be operated by advanced users having thorough knowledge of video equipment.
	SW3-7 : Not used	
	SW3-8 : Not used	

Table 3-1-2

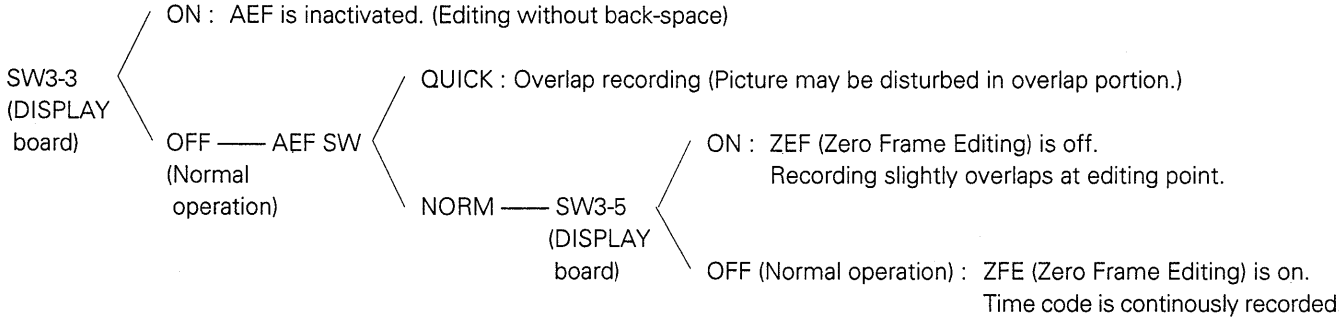

SW3-3
(DISPLAY
board)
ON : AEF is inactivated. (Editing without back-space)
OFF (Normal operation)
AEF SW
QUICK : Overlap recording (Picture may be disturbed in overlap portion.)
NORM
SW3-5
(DISPLAY
board)
ON : ZEF (Zero Frame Editing) is off.
Recording slightly overlaps at editing point.
OFF (Normal operation) : ZFE (Zero Frame Editing) is on.
Time code is continously recorded.

Fig. 3-1-5 AEF setting chart

Switch position		Back-space	Review	Zero Frame Editing	Overlap
AEF switch	REVIEW switch				
NORM	ON	3.9 sec approx.	2.4 sec approx.	ON	0 frame
NORM	OFF	2.0 sec approx.	0 sec	ON	0 frame
QUICK	ON	3.3 sec approx.	2.4 sec approx.	OFF	5 to 7 frames
QUICK	OFF	1.3 sec approx.	0 sec	OFF	5 to 7 frames

Table 3-1-3 AEF/Auto review functions

3.1.5 Tape protection function

- STILL mode

Time lapse	Tape transport condition
3 minutes 30 seconds	Tape is forwarded for several frames.
7 minutes 30 seconds	Tape is forwarded for several frames.
10 minutes 30 seconds	STOP mode (Unloading condition)

- INSERT PAUSE mode

Time lapse	Tape transport condition
10 minutes 30 seconds	STOP mode (Unloading condition)

- REC PAUSE mode

Time lapse	Tape transport condition
10 minutes 30 seconds	Tape is shifted to the REC LOCK position (tape tension is slightly decreased).
10 ± 1 minutes	Drum stops (left in the loading condition).

3.2 SERVO CIRCUIT

3.2.1 IC7 (BU5753S) block diagram

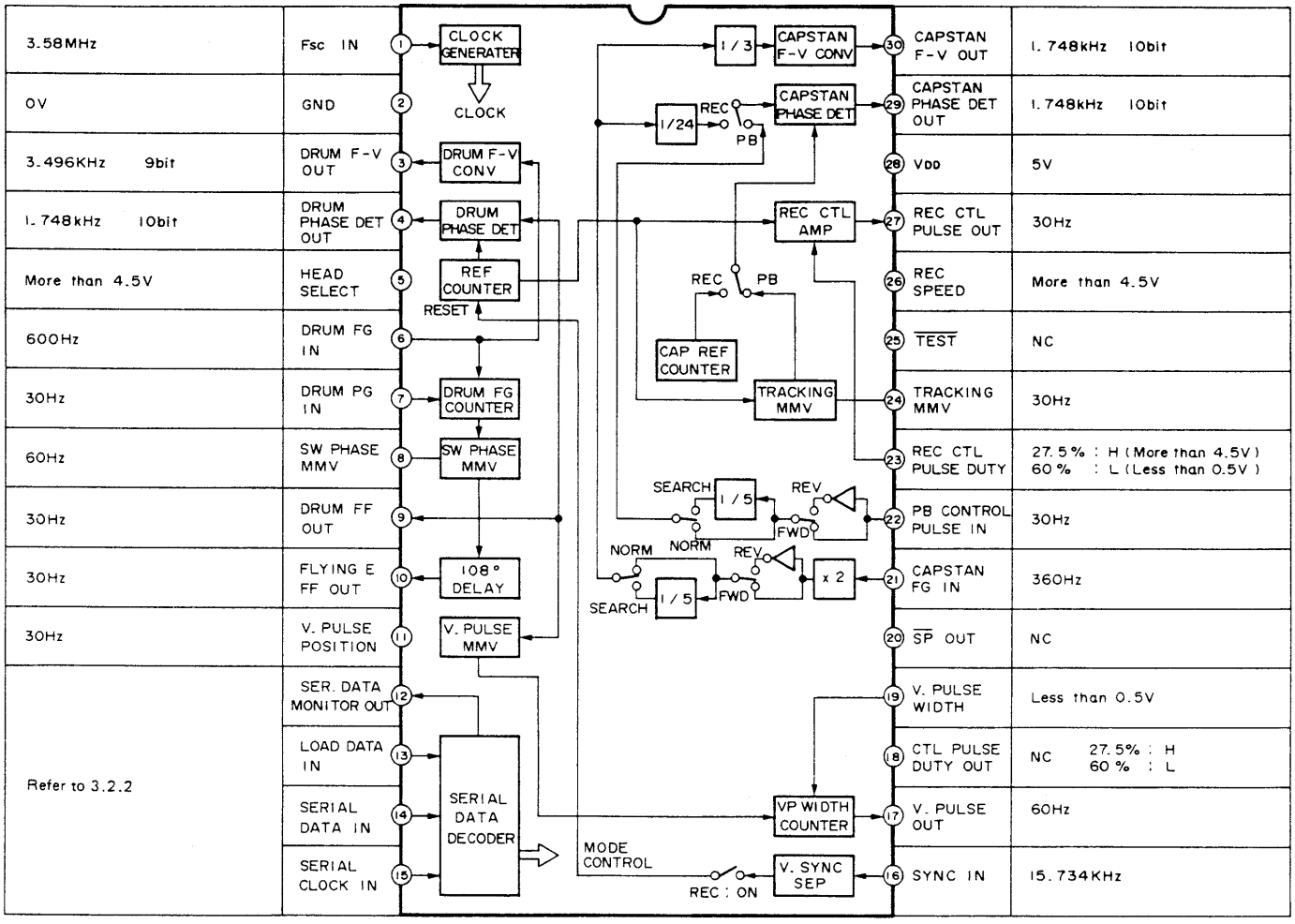


Fig. 3-2-1 Servo circuit block diagram

3.2.2 IC7 serial data timing chart

IC17 of the S/S board controls IC7 of the SERVO board with serial data signal.

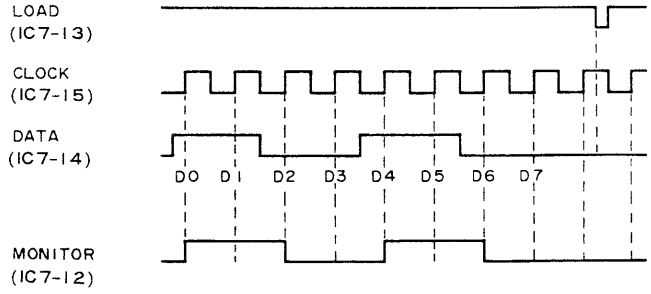


Fig. 3-2-2

● Serial data

Mode	D0	D1	D2	D3	D4	D5	D6	D7
REC	1	1	0	0	0	0	0	0
INST	0	1	0	0	0	0	0	0
PB	0	0	0	0	0	0	0	0
REV PB	0	0	1	1	1	0	0	0
SEARCH FWD	0	0	0	1	0	1	0	1
SEARCH REV	0	0	1	1	0	1	0	1
STILL	0	0	0	0	0	1	1	1
REC PAUSE	1	0	0	0	0	0	0	0

3.2.3 Servo timing chart

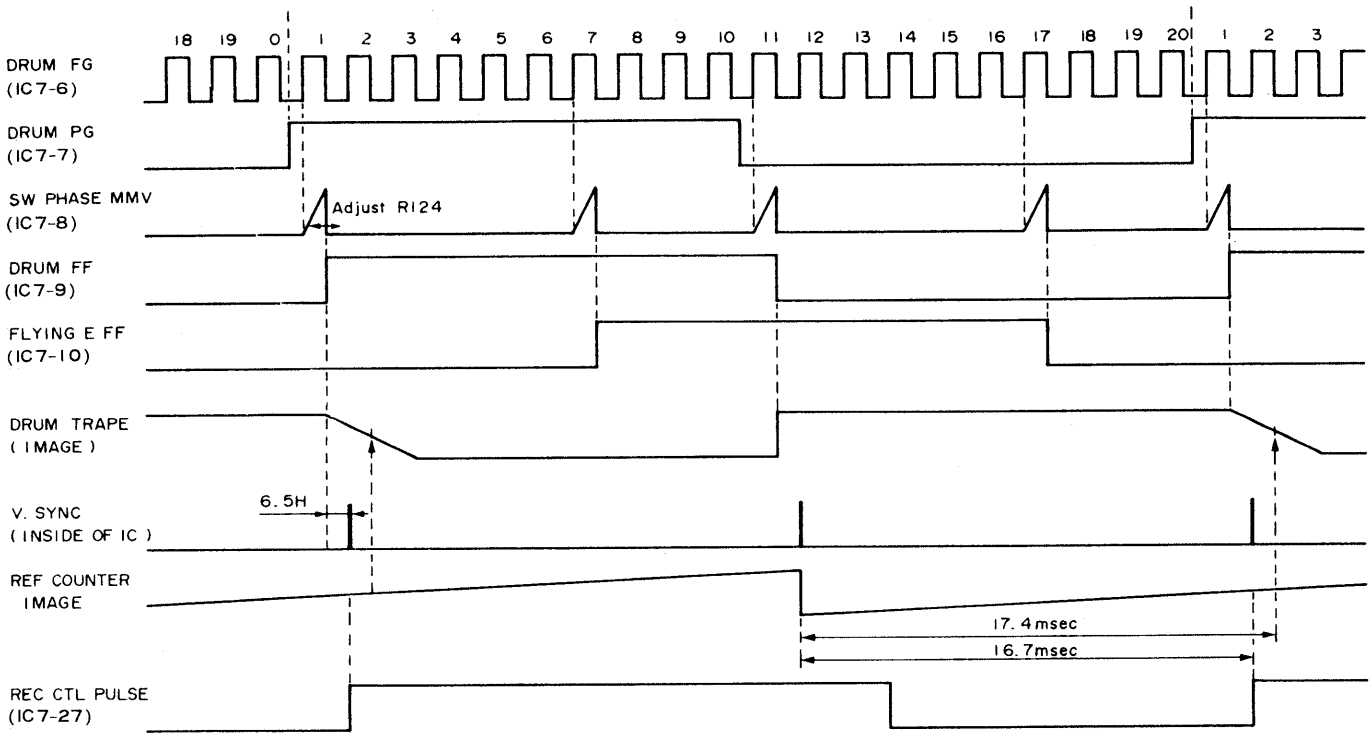

18 19 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 1 2 3
DRUM FG (IC7-6)
DRUM PG (IC7-7)
SW PHASE MMV (IC7-8)
Adjust R124
DRUM FF (IC7-9)
FLYING E FF (IC7-10)
DRUM TRAPE (IMAGE)
6.5H
V. SYNC (INSIDE OF IC)
REF COUNTER IMAGE
17.4msec
16.7msec
REC CTL PULSE (IC7-27)

Fig. 3-2-3 Drum servo timing chart

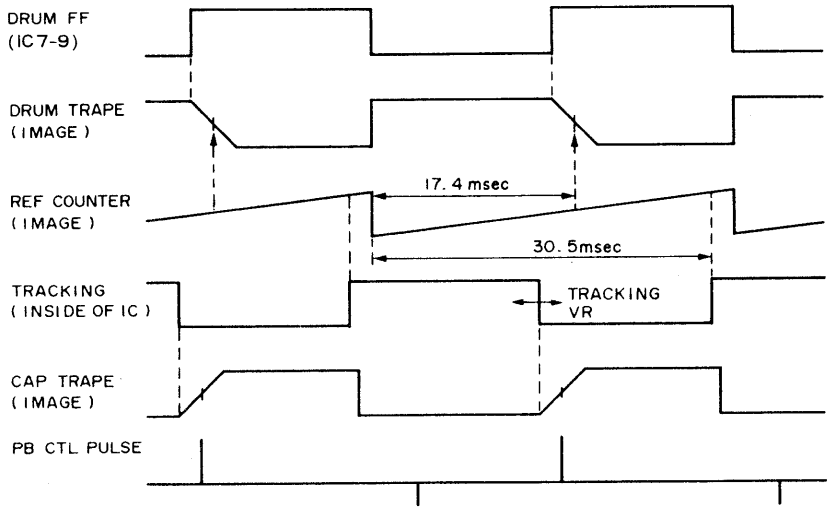


Fig. 3-2-4 Playback servo timing chart

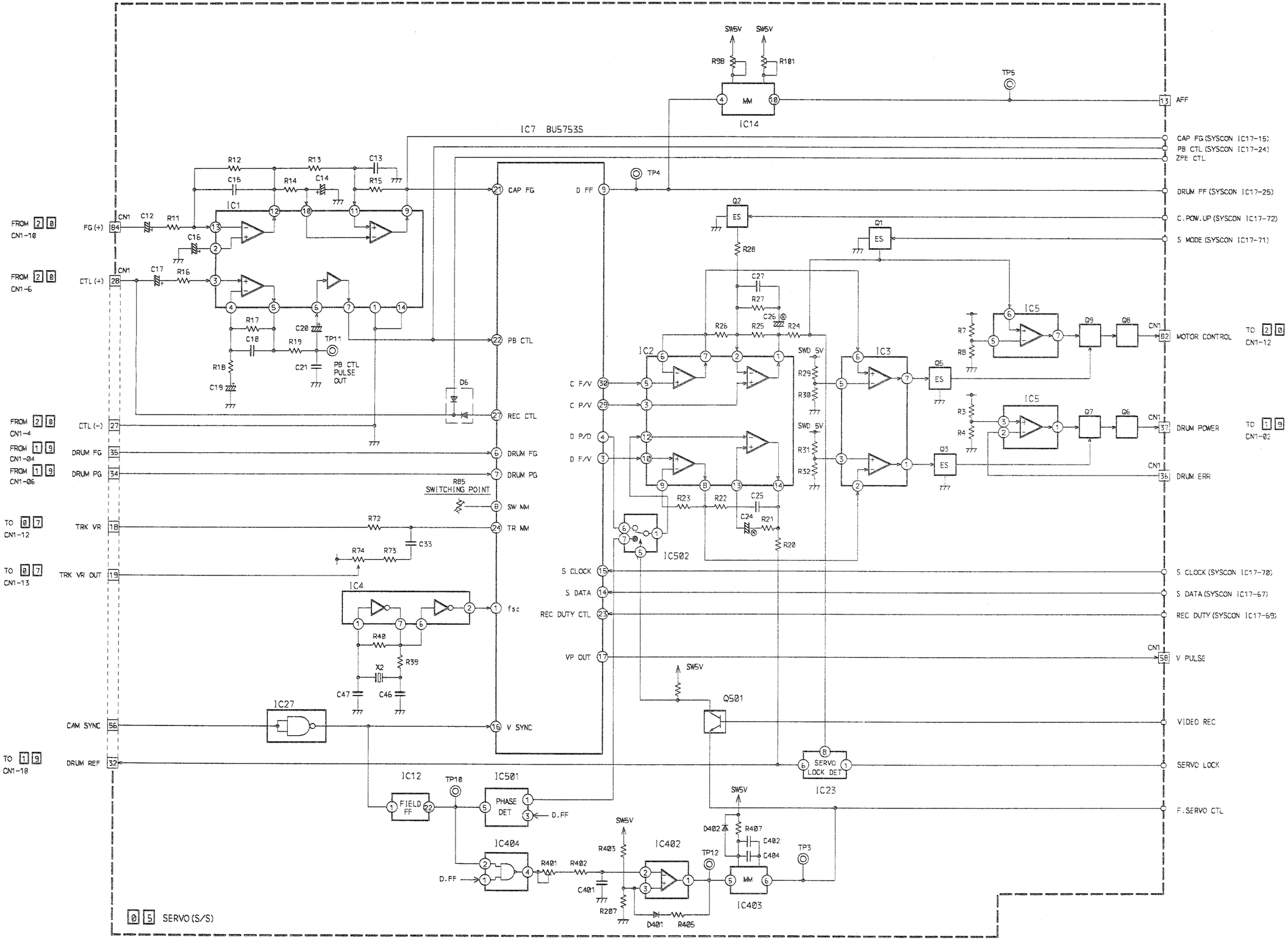


Fig. 3-2-5 Servo circuit block diagram

3.2.4 Zero frame editing

In this model the duty of the CTL pulse is controlled for smooth splicing of pictures in the zero frame editing. At the end of a recording ZFE (ZERO FRAME EDIT) pulse is written on the tape and it will be read out at the editing point in the preroll operation in order to continue pictures before and after the editing point smoothly.

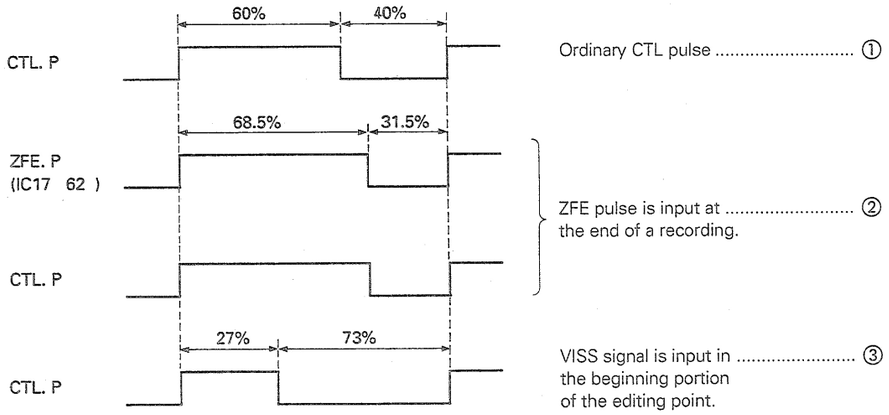


Fig. 3-2-6 CTL pulse duty

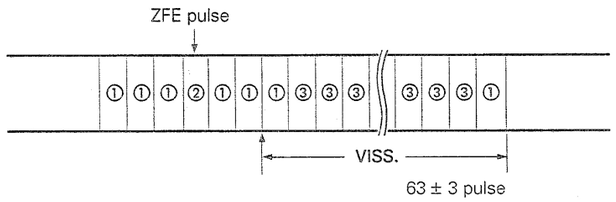


Fig. 3-2-7 Edit mode control pulse

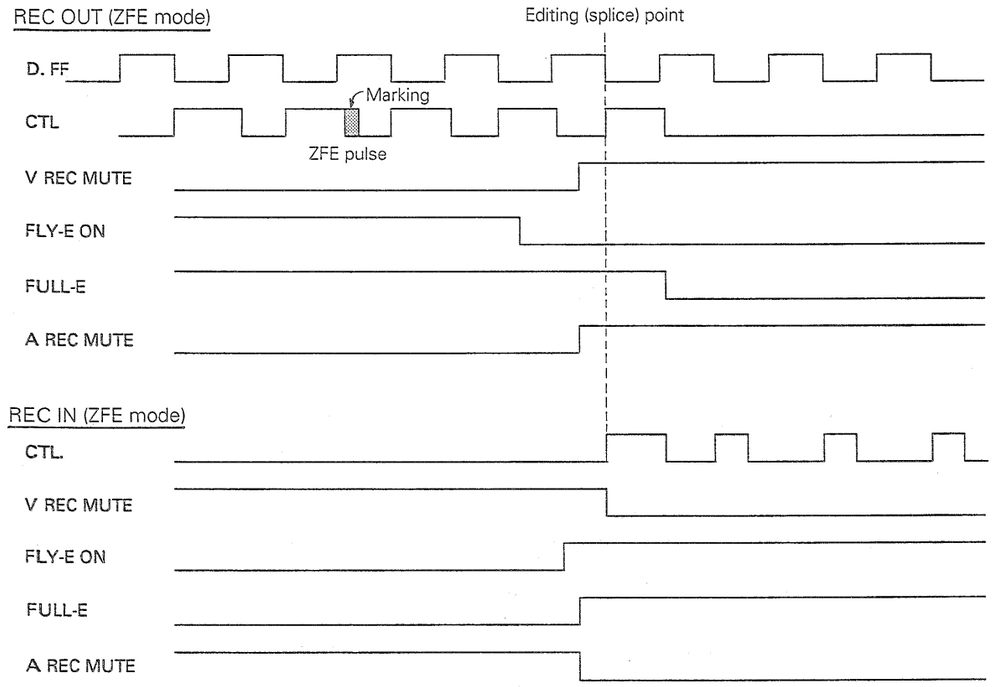


Fig. 3-2-8 Blanking switch timing

3.2.5 Control of frame servo

In recording the frame servo is controlled by controlling the DRUM PHASE DET signal (IC7 pin ④).
V. sync signal that underwent synchronizing separation is input to IC12 of the S/S board. IC12 is a frame detector, which generates FIELD FF waveform.

The phase of the FIELD FF is compared with that of the DRUM FF by IC501. When the phase of the FIELD FF is in advance of the DRUM FF's phase, IC501 pin ① outputs "H" to IC502, while it outputs "L" when the DRUM FF advances in the phase.

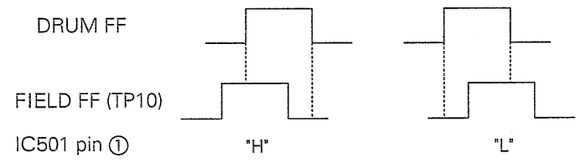


Fig. 3-2-9

IC404, IC402, IC403 detect whether the frame servo is locked or not in order to change over the switch of IC502, namely, when the frame servo is locked, "H" is output from TP3, while "L" is output when it is not locked.

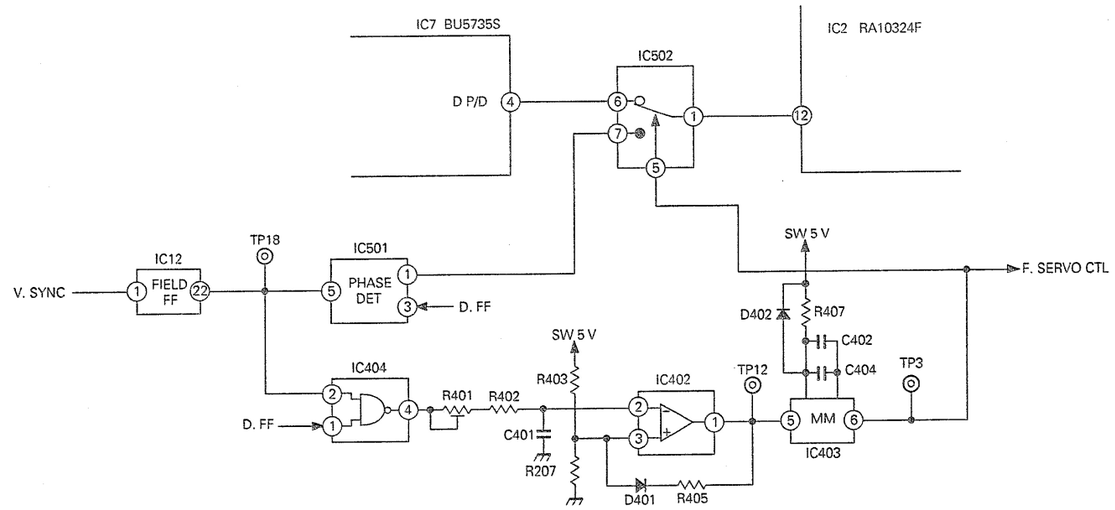


Fig. 3-2-10 Frame servo circuit

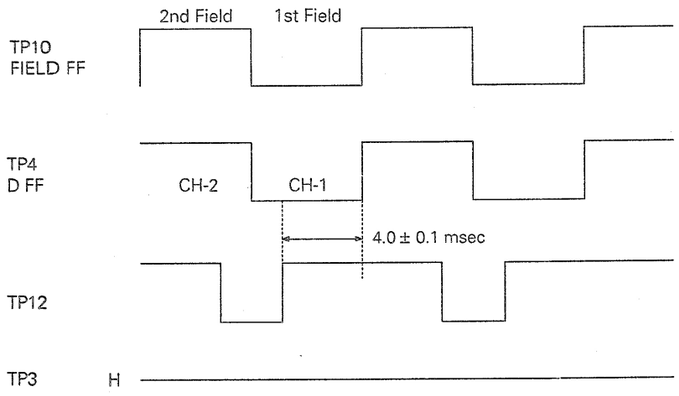


Fig. 3-2-11 Timing chart when frame servo is locked

3-10

SECTION 4
VIDEO CIRCUIT

● **DIFFERENCE BETWEEN BR-S422 AND BR-S411**

Different points	BR-S411B	BR-S422
EE output	Passes AGC circuit.	Does not pass AGC circuit.
AUTO EQ circuit	×	Adds reference signal in recording. Does not functions as AUTO EQ circuit in playback. Does not get reference signal blank.
Y signal S/N ratio improvement	By ordinal noise canceller	By new noise canceller utilizing advance limiter.
Color signal S/N ratio improvement	By ADV. REC circuit	Z circuit (Amplifies low level color signal for recording as well as the ADV. REC circuit.)

● REC mode

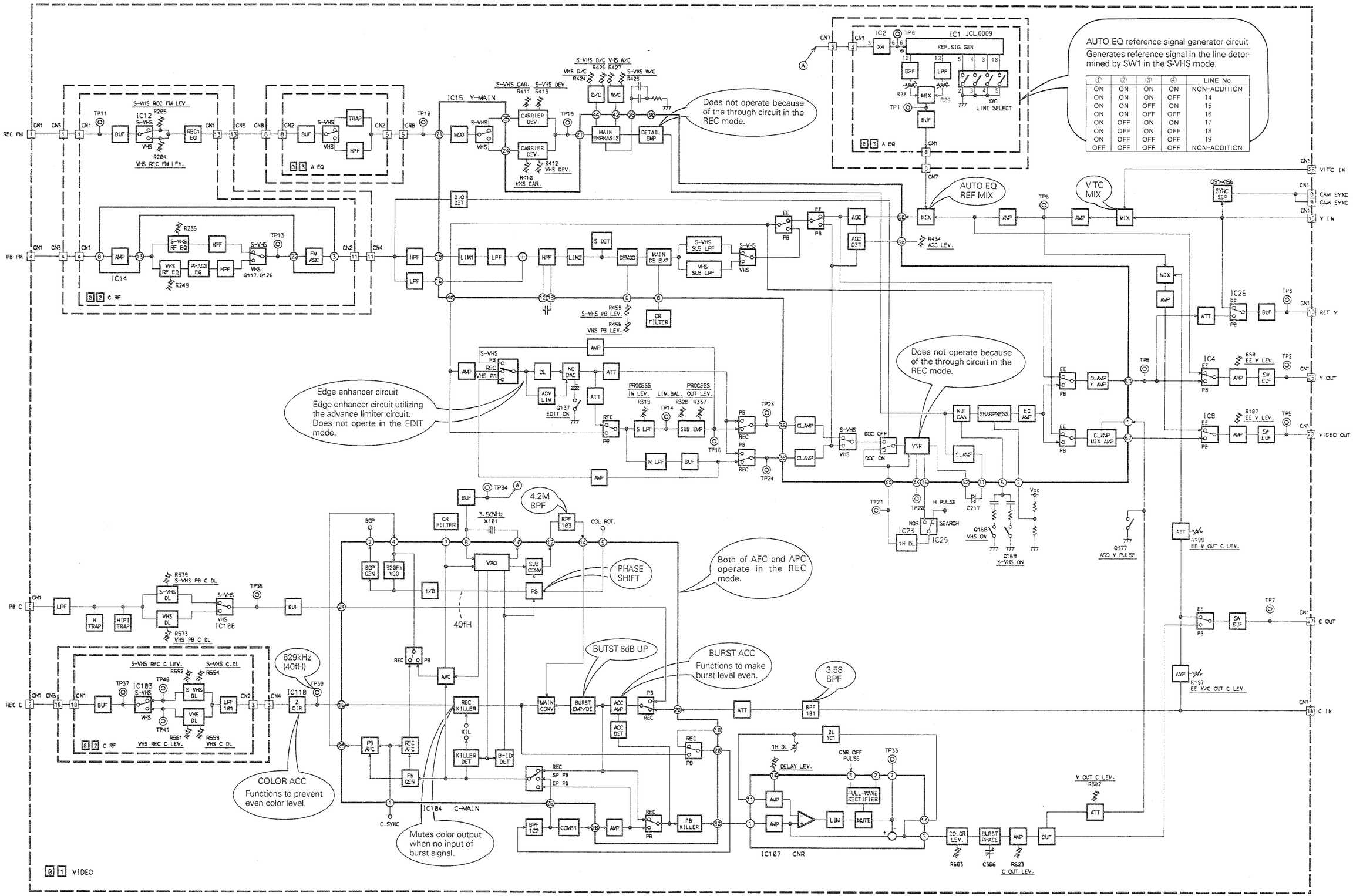


Fig. 4-1-1

● PB mode

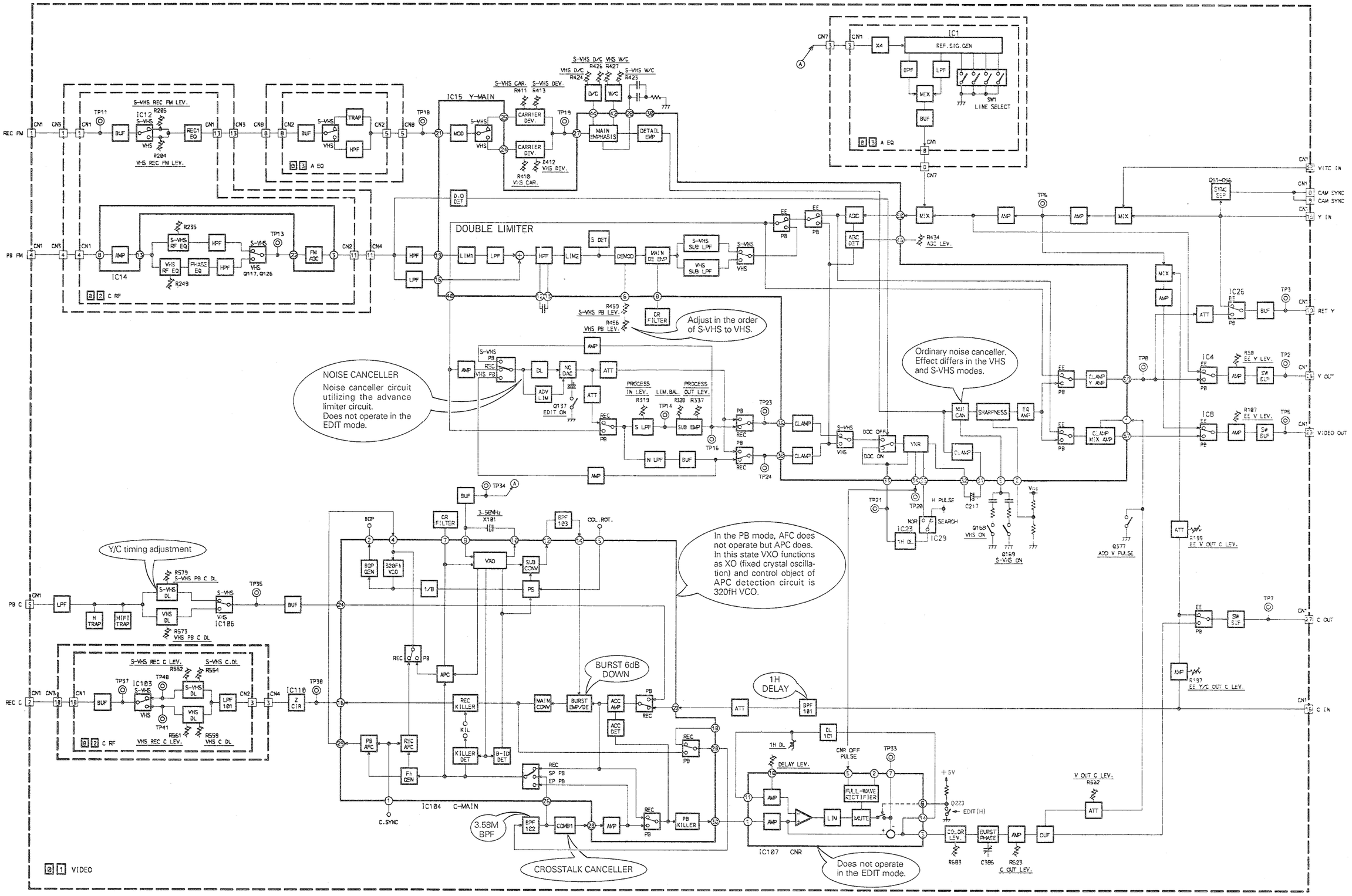


Fig. 4-1-2

4.1 Y (LUMINANCE) SIGNAL SYSTEM

4.1.1 VITC MIX circuit

When the TIME CODE board is incorporated in the VTR, this circuit mixes VITC (Vertical Interval Time Code) signal in the V. blanking period. One line comprises of 90 bits and the signal is mixed in two lines of the 16H and 18H lines in the initial setting mode.

4.1.2 AUTO EQ MIX circuit

This circuit mixes reference signal supplied from the AUTO EQ board. In the initial setting, reference signal is mixed in 17 lines only in the S-VHS mode.

- Outline of AUTO EQ circuit

The AUTO EQ circuit is installed to prevent frequency response from deterioration caused by demagnetization of tape and to control irregularity in respective frequency characteristics of tapes used. Two reference signals of 629 kHz and 3.58 MHz are recorded in optional lines in the V. blanking period, and the video equalizer is controlled in playback to equalize PB level of each reference signal with that of the original. Accordingly, the frequency response is automatically adjusted in the S-VHS mode.

This VTR is designed to be used as a recorder, therefore, it adds reference signal but has not equipped with any automatic PB adjusting circuit. In case of the BR-S822, it gets AUTO EQ reference signal blank in video output, however, the BR-S422 does not blank the reference signal and outputs it as it is added.

- Reference signal generator circuit

Reference signals are generated by the gate array IC (IC1, JCL0009). This IC receives 4 fsc clock through the pin ⑥ while it receives sync. signal through the pin ⑳, and it outputs 629 kHz reference signal through the pin ⑬ while 3.58 MHz reference signal through the pin ⑫. These reference signals are supplied to the LPF and BPF circuits which mix them to be output as the reference signal synchronizing with the sync. signal.

Pins ③, ④ and ⑤ function to control the reference signal insertion line which is selected by SW1. In detail, line selection is performed by SW1-2, SW1-3 and SW1-4, and, when all of them are on, nothing is selectd for insertion. If SW1-1 is off, the SW 5V signal line of the circuit is cut off, therefore insertion is not activated without change of the insertion lines set by SW1-2, -3 and -4.

R29 and R38 are variable resistors to adjust reference signal level so that the ratio between sync. level, 3.58 MHz level and 629 kHz level becomes 4 : 3.4 : 3.6 since this VTR has not the playback circuit for automatic level adjustment. (For a reference, the BR-S822 records sweep signal and plays it back to obtain the specific frequency response.) The above-mentioned ratio is determined to obtain the specific frequency response on the condition that the BR-S422 is used for recording and the BR-S822 for playback.

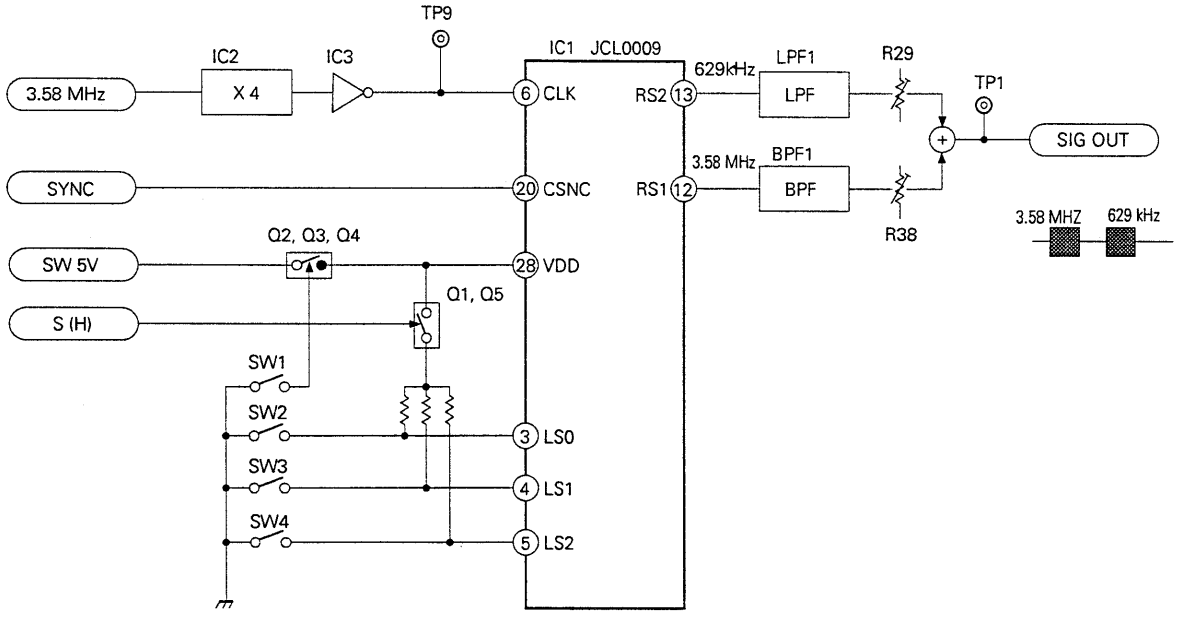


Fig. 4-1-3

4.1.3 NC/DAC (Noise Canceller/Dynamic Aperture Control) circuit

The circuit shown as NC/DAC in the block diagram is a new noice canceller/dynamic aperture control (NC/DAC) circuit employing the advanced limiter circuuit, and it functions as the edge enhancer circuit in recording while it does as the noice canceller circuit in playback.

The advance limiter circuit realizes the input/output characteristic shown in Fig. 4-1-4 by combining a differential amp. (IC17) and a limiter (IC18).

As the edge enhancer, this circuit hardly influences the frequency response of comparatively high amplitude signal. Therefore, enhancement in thin and light portions is visually the same as the effect of ordinary detail enhancers without emphasis in high amplitude portions, and picture is consequently natural.

As the noise canceller, it does not deteriorate high amplitude signal in the frequency response since it takes reverse operation of the edge enhancer. As a result, this circuit performs clear edge enhancement without getting picture unsightly owing to its function to cancel low level noise only.

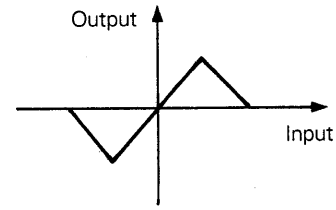


Fig. 4-1-4

- Edge enhancer circuit

In recording the NC/DAC circuit is supplied with luminance signal of 1.5 Vp-p. At that time, Q136 is off and Q134 is on since the level of PB(H) signal is "L". Therefore, the differential amp. inside the advance limiter circuit and the LPF circuit composed of C151 and R287 construct an HPF circuit whose cutoff frequency is 1 MHz. Inside the limiter circuit, only the low level components (under 4 IRE approximately) of the output of the HPF are output in the same phase as that of the input signal. Finally, this output is mixed with luminance signal that is delayed for the delay time (50 ns) of the limiter circuit, therefore, the circuit functions as the edge enhancer circuit excent in the EDIT mode because Q137 is on in the EDIT mode.

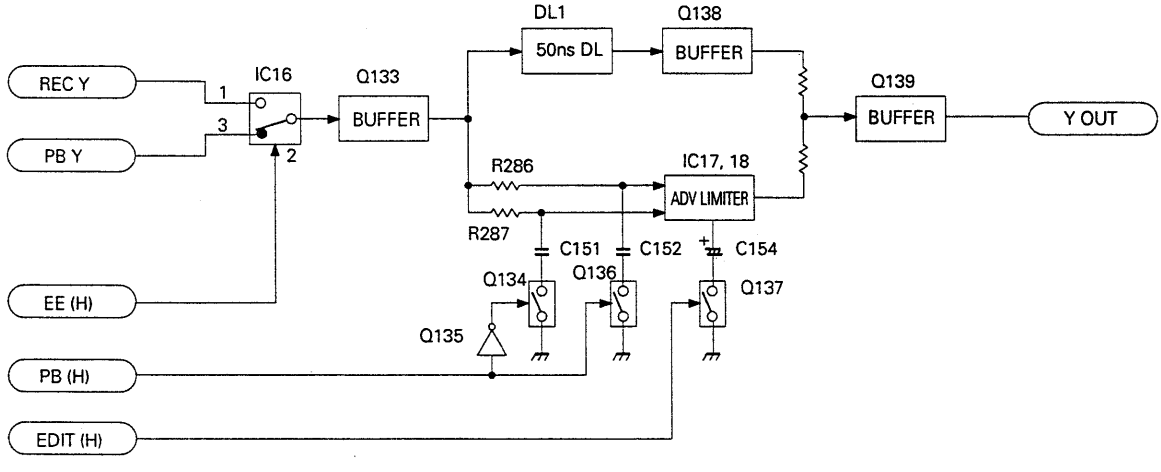


Fig. 4-1-5 Edge enhancer/noise canceller circuit

- Noise canceller circuit

In playback the NC/DAC circuit is supplied with luminance signal of 2.0 Vp-p. At that time, Q134 is off and Q136 is on since the level of PB(H) signal is "H". Therefore, the LPF circuit composed of C152 and R286 and the differential amp. inside the advance limiter circuit function as the HPF circuit as same as it functions as the edge enhancer circuit. However, output of the HPF circuit has the reverse phase of that in the condition of the edge enhancer circuit, and the output of the limiter circuit consequently has the reverse phase of the input signal. As a result, the circuit functions as the noice canceller circuit.

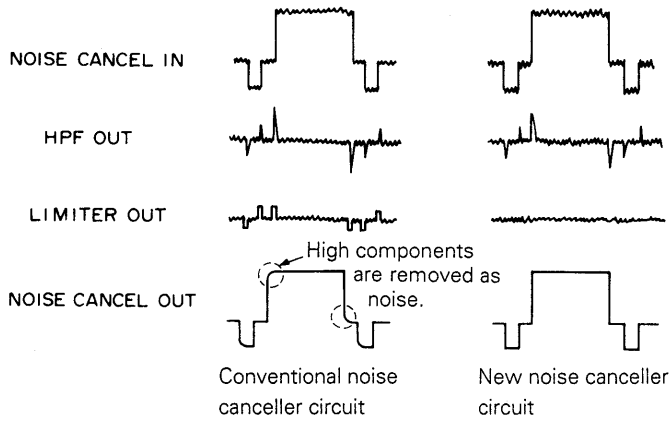


Fig. 4-1-6 Noise canceller circuit

4.1.4 YNR/DOC circuit (IC15)

In IC15, the YNR block functions only to generate non-correlative pulse and the noise reduction circuit is not activated. Therefore, this IC is used to detect non-correlation between 1H delayed PB Y signal and DOC compensation signal.

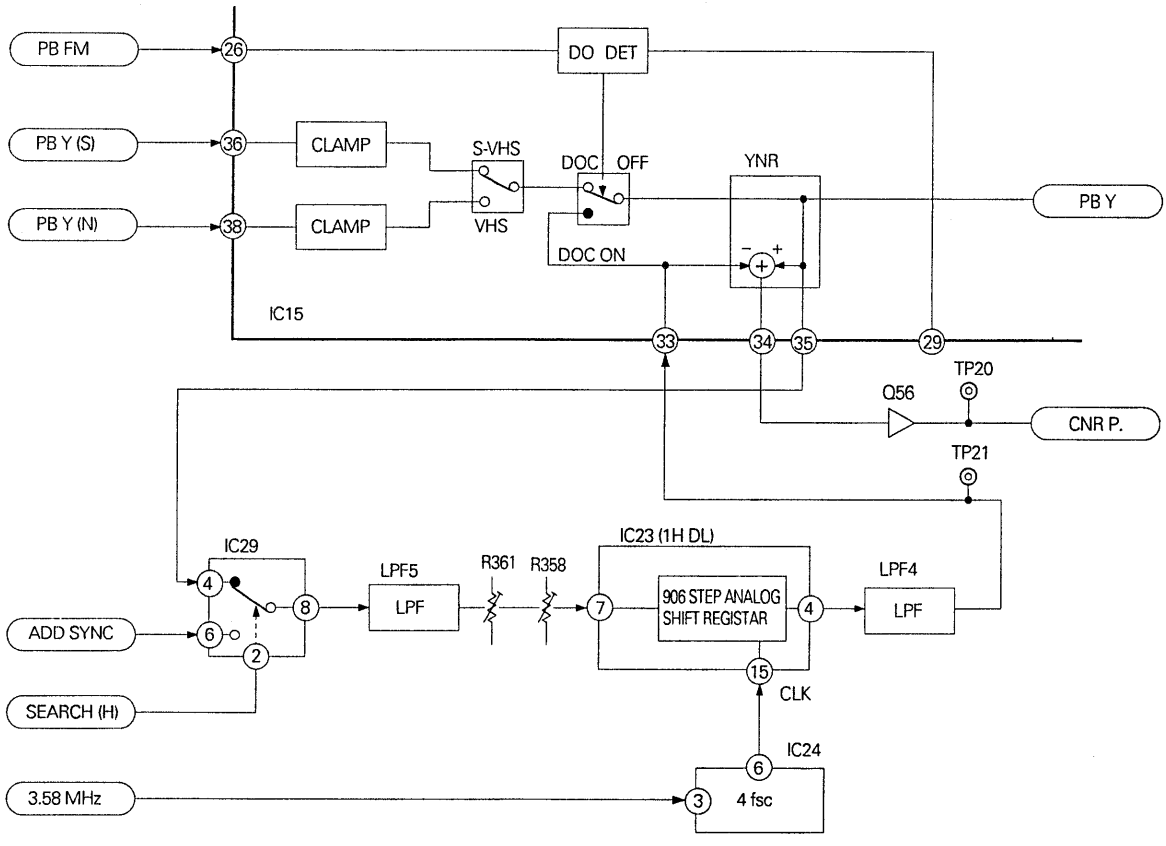


Fig. 4-1-7

- Detection of non-correlation

PB Y signal undergoes subtraction from 1H delayed Y signal and the resultant signal becomes CNR P (non-correlative Y pulse) and is output from pin 34 of IC15 to the CNR circuit. 1H delay of Y signal is performed by IC23 (MN3801S) with the additional filter (LPF4) outside the IC23 by sampling it with clock input whose frequency (14.32 MHz) is 4 times as high as the color subcarrier.

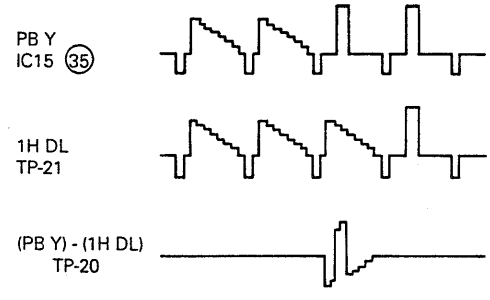


Fig. 4-1-8

• DOC circuit

When signal dropout occurs, this circuit compensates it by replacing dropout portion with the signal of 1H before. In the Search mode it inserts sync signal into dropout portion. This circuit also functions to mask noise bar in the monitor screen. (Fig. 4-1-9).

In the Search mode, switching to ADD SYNC signal is operated by IC29.

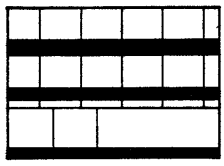


Fig. 4-1-9

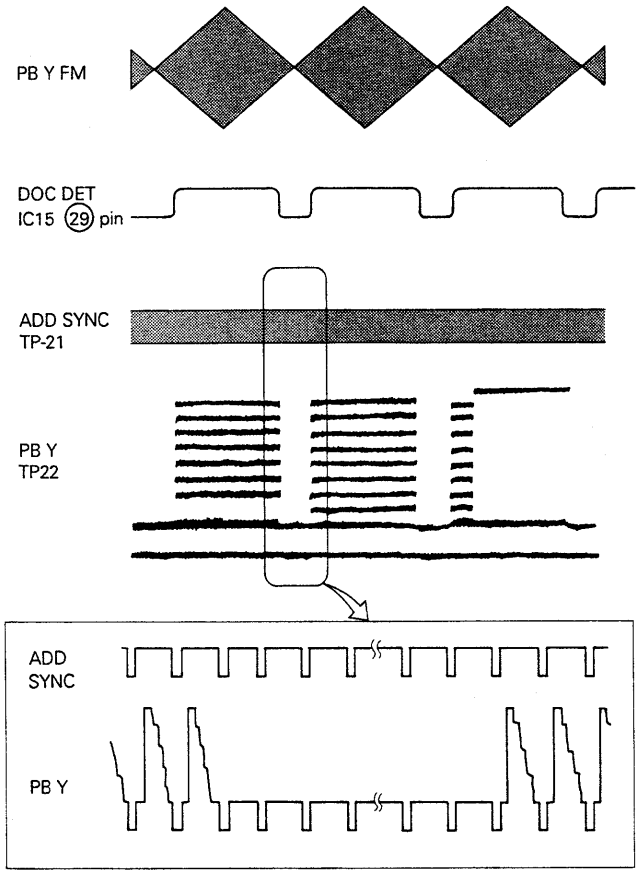


Fig. 4-1-10 Dropout compensation in Search mode

4.1.5 TRAP/HPF circuit (AEQ board)

The TRAP/HPF circuit removes FM luminance signal's sideband existing in low frequency (629 ± 500 kHz) where low-converted color signal is duplexed and reduces cross color as well. The trap frequency is 715 kHz, since the side of +500 kHz of the 629 ± 500 kHz low color band is interfered by the sideband of Y signal. From this reason, the trap frequency is set to 715 kHz that is higher than 629 kHz.

The –3 dB cutoff frequency of the HPF is 1.1 MHz.

4.1.6 Double limiter circuit (IC15)

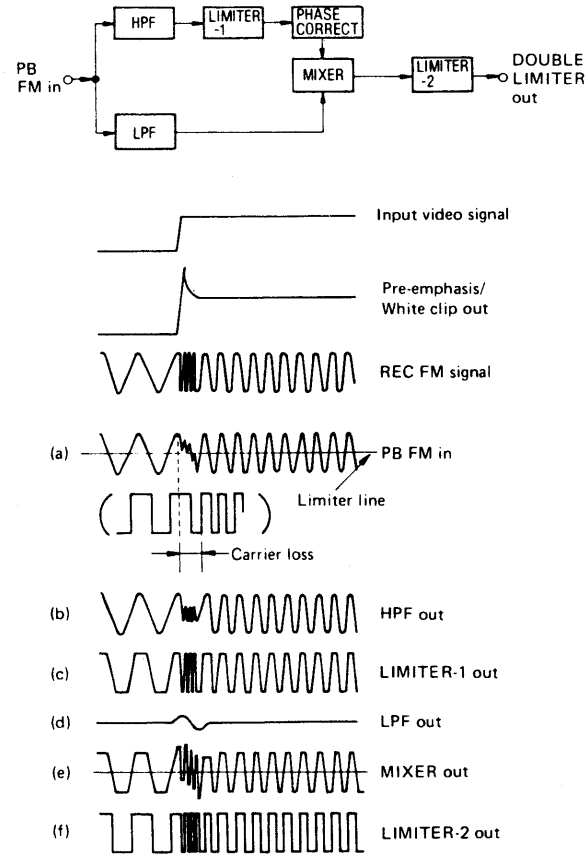


Fig. 4-1-11 Double limiter circuit

When pre-emphasis is applied to the portion where AM signal varies black level to white level, it result in overshoot. The waveform (a) in the above figure shows the playback signal of that portion. If that signal is limited by the center limiter line, the limiting has no effect on the carrier dropout portion and black/white reversal and impaired S/N may occur. Therefore, the signal is supplied to the HPF and LPF circuits to divide into carrier components and low sideband components, which are shown by the waveforms (b) and (d). The signal that passed the HPF is supplied to the limiter-1 to have the limiter gain of 10 dB approximately, and then it is supplied to the mixer, which mixes two signals coming from the HPF and LPF. The mixed signal is supplied to the limiter-2. The waveform of this signal is shown as the waveform (e).

The phase corrector circuit functions just for phase adjustment. In other words, it limits the signal without losing importrant information of the low sideband components. And, the double limiter, which corrects the ratio between the carrier and the sideband without amplification of noise components, prevents the signal not only from carrier dropout caused by pre-emphasis but also from black and white reversal. As a result, adequate pre-emphasis can be applied to the signal and the S/N ratio at the high frequency is accordingly improved.

4.2 COLOR SIGNAL RECORDING SYSTEM

4.2.1 BPF101 (Band Pass Filter 101)

The BPF101 whose band width is 3.58 MHz ± 500 kHz extracts color signal from input video signal.

4.2.2 ACC (Automatic Chroma Level Control) circuit

The ACC circuit automatically adjusts the color signal level to the predetermined value.
The ACC extracts only the burst signal to sense the level and controls the gain to make it constant.
In general, burst signal level is constant when there is no amplitude distortion in the transmission system, therefore, it can be said that this circuit eliminates amplitude distortion in the transmission system.

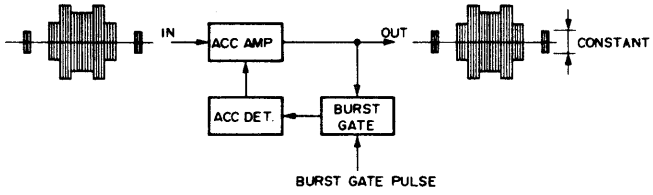


Fig. 4-2-1 ACC block

4.2.3 Burst emphasis circuit

In the VTR of the VHS format, burst signal level is increased double (6 dB) to improve the S/N ratio of the burst signal for the purpose of reducing irregularity in color and transversal noise in recording signal on the tape and playback of the recorded signal.

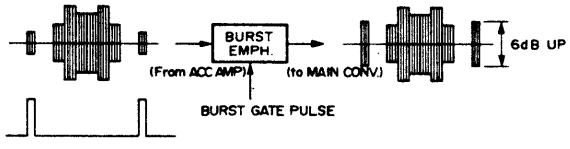


Fig. 4-2-2 Burst emphasis

4.2.4 Main converter

The main converter functions to convert Fs (3.57945 MHz) color signal into 40 Fh (629.371 kHz) signal. Besides color signal there is Fs + 40 Fh signal supplied to the main converter, therefore, it outputs 2 Fs + 40 Fh signal of the sum component and 40 Fh signal of the difference component.

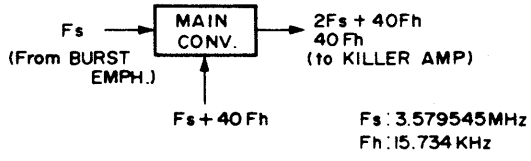


Fig. 4-2-3 Main converter

4.2.5 Color killer circuit

The color killer circuit cuts the color signal when B/W TV signal is input.
This circuit gets the 3.58 MHz VCO to oscillate synchronously with input burst signal. If it synchronously oscillates, the input signal is color TV signal. For detection of synchronous oscillation, this circuit compares the phases of two signals, one is the signal that the 3.58 MHz VCO output is shifted in the phase at an angle of 90° and the other is the input burst signal.

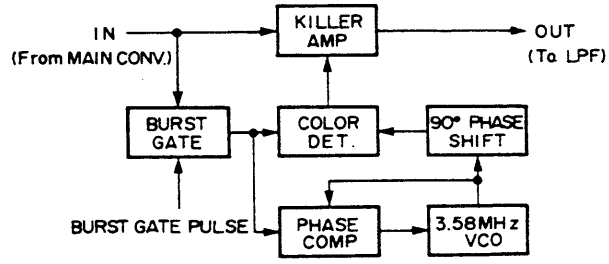


Fig. 4-2-4 Color killer circuit

4.2.6 LPF101 (Low Pass Filter 101) (C RF board)

The output of the main converter contains 2 Fs + 40 Fh signal of the sub component besides the low-converted color signal of the necessary difference component. Therefore, the LPF circuit removes undesirable sum components.

4.2.7 APC (Automatic Phase Control) circuit

The APC circuit compares the burst signal of the input color signal that is the reference signal and the output signal of the 3.58 MHz VCO that is the comparison signal in the phase with the BURST GATE pulse in order to control the 3.58 MHz VCO. Therefore, a 3.58 MHz signal whose phase is the same as that of the input color signal is supplied to the subconverter.

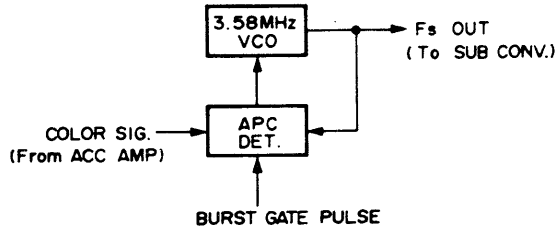


Fig. 4-2-5 REC APC block

4.2.8 AFC (Automatic Frequency Control) circuit

The AFC circuit functions as follows.

1. Generates 40 Fh (629.36 kHz) signal.
2. Shifts the 40 Fh signal at an angle of 90° every 1 H.
3. Corrects the phase with H. sync signal.

Refer to Fig. 4-2-6.
H. sync signal is supplied from the Y circuit to the 1/2H pulse killer that cuts the 1/2H sync signal of the V. sync signal portion, then it is further supplied to the AFC detector and the phase converter.

The AFC detector is the phase comparator circuit of the AFC loop, and its reference signal is the H. sync signal while its comparison signal is the Fh signal that the 320 Fh VCO output is divided to 1/320.
Error output of the AFC detector is supplied to the 320 Fh VCO, which accordingly oscillates at 320 Fh (5.035 MHz). This 320 Fh signal is divided half, then it is supplied to the phase converter, to which DRUM FF signal and H. sync signal are supplied besides the half-divided 320 Fh signal.
The output of the phase converter is 40 Fh signal, and the phase of the signal recorded by the CH-1 video head is advanced at an angle of 90° every 1 H while the phase of the signal recorded by the CH-2 head is delayed at an angle of 90° every 1 H. The 40 Fh signal is supplied to the subconverter as the AFC output.

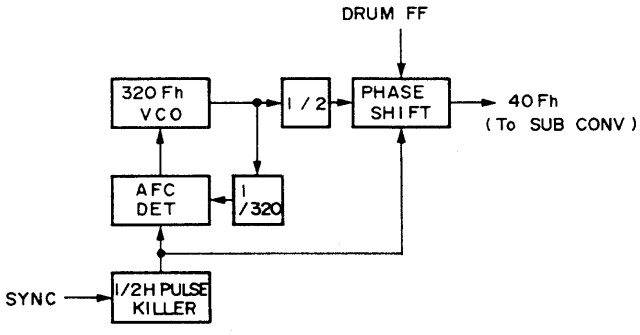


Fig. 4-2-6 REC AFC block

4.2.9 Subconverter and BPF103

The subconverter converts the Fs (3.579545 MHz) signal into Fs + 40 Fh signal. Besides the Fs signal, the subconverter is supplied with 40 Fh signal, therefore, it outputs the Fs + 40 Fh signal of the sum component and the Fs – 40 Fh signal of the difference component.
The BPF103 extracts the necessary Fs + 40 Fh signal while it cuts off the undesirable Fs + 40 Fh signal.

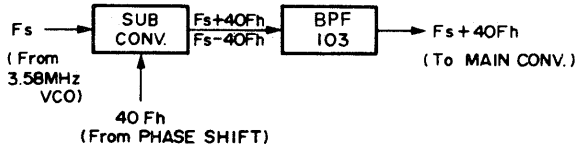


Fig. 4-2-7 Subconverter and BPF103

4.2.10 Burst gate pulse generator

The burst gate pulse generator which is supplied with the 320 Fh signal and H. sync signal generates BURST GATE pulse by counting the 320 Fh signal according to the H. sync signal as the reference.

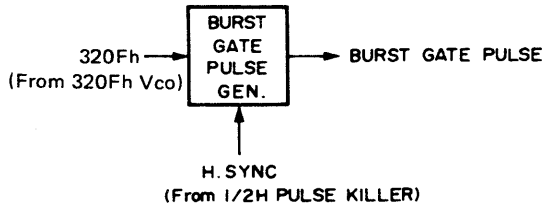


Fig. 4-2-8 Burst gate pulse generator

4.2.11 Z circuit (IC110, AN6366N)

This VTR incorporates the Z circuit as the color ACC circuit to amplify low level color signal together with burst signal in the recording color signal processing circuit besides the ordinary burst ACC circuit to make the burst signal level constant.
The level of low level color signal that is amplified by the Z circuit is restored to the original level by the burst ACC in playback, therefore, noise component is reduced in that process and the S/N ratio is consequently improved. The basic idea of this circuit is the same as the ALU (Automatic Level Up) circuit employed in the BR-S822 whose ALU circuit changes the rate of amplification of color signal according to the volume of the sideband in the FM signal. However, the Z circuit of this model does not operate such variable amplification.

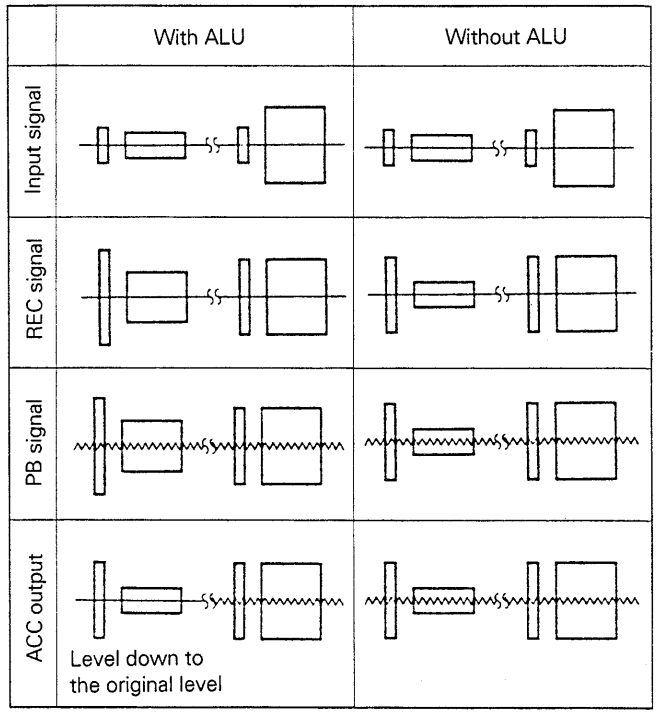


Fig. 4-2-9 Principle of ALU cirdcuit

The IC AN6366N whose block diagram is shown in Fig. 4-2-10 performs the automatic chroma level control for the color signal. This IC is capable of operating as the burst ACC circuit, but it functions as the color ACC circuit of the recording system in this VTR.

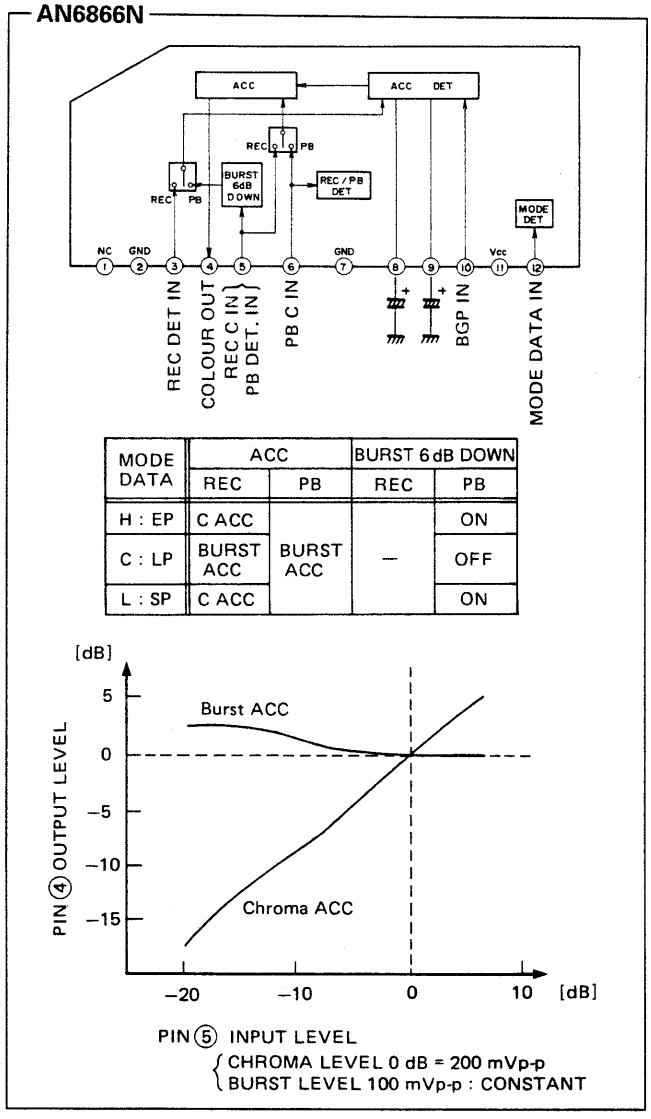


Fig. 4-2-10 PB color signal processing block

4.3 COLOR SIGNAL PLAYBACK SYSTEM

4.3.1 LPF102

LPF102 extracts low-converted color signal from playback signal and attenuates undesirable luminance component.

4.3.2 H trap/Hi-Fi trap circuit

This circuit reduces nuisance signal coming from the servo system and interference of Hi-Fi carrier. The trap frequencies are 15.7 kHz and 1.4 MHz.

4.3.3 ACC circuit

As well as in recording, the ACC circuit extracts burst signal and controls the gain of color signal so that the burst signal level is always constant.

4.3.4 Burst de-emphasis circuit

This circuit restores burst signal level that is increased by 6 dB in recording to the original level.

4.3.5 Main converter and BPF102

The main converter is supplied with the Fs + 40 Fh signal from the subconverter as same as in recording, and it outputs the original Fs color signal since it gets the input signal to pass the BPF102 before output.
In actual, playback color signal contains various fluctuations (in frequency and phase) resulting from change of the tape speed, irregular rotation of the video head, expansion and contraction of the tape, etc. For correction of such the fluctuation, refer to the description about the APC circuit.

4.3.6 Comb 1 (crosstalk canceller)

Since low-converted PB color signal which is processed by phase shift has has a relation reverse to the signal 1H before in the crosstalk with the neighboring track, the signal is added with another signal that passed the 1H delay line to increase the signal level double. Accordingly, crosstalk is mostly removed for the reason that the two signals cancel the crosstalk each other.

4.3.7 Color killer circuit

This circuit functions to cut color signal output when playback signal is B/W signal. The operation is the same as in the recording.

4.3.8 Correction of frequency and phase change

When played back low-converted color burst signal is regarded as Fsc', the Fsc' is explained by the following equation.

$$Fsc' = 40\,Fh' \pm \Delta f,$$

wherein Fh' expresses change of frequency caused by change in the tape speed and it is corrected by the AFC circuit, while $\pm\Delta f$ expresses change of phase caused by irregular rotation of the video head and expansion and contraction of the tape and it is corrected by the APC circuit.

In normal playback correction is made by the APC circuit only, and the frequency detection circuit is activated only when the frequency exceeds the locking range of the APC circuit and controls the frequency change to be within the locking range of the APC.
The APC circuit is explained first.
The reference signal of the APC circuit is the Fs signal that is output from the 3.58 MHz VCO. And, its comparison signal is playback color signal.
The PB APC detector extracts burst signal from the playback color signal with the burst gate pulse and detects its phase difference (±Δf) from the Fs signal. This phase difference is supplied to the 320 Fh VCO as the error voltage.
Next, the frequency detection circuit is explained.
The frequency detection circuit judges whether the oscillation frequency Fvco of the 320 Fh VCO is within (320 – 1.25)Fh < Fvco < (320 + 1.5) Fh at an interval of 8H period.
The frequency detector normally outputs high impedance pulse, but it outputs high potential pulse every 8H when the frequency is low, while it outputs low potential pulse every 8H when the frequench is high. Therefore, the frequency detector supplies error voltage equivalent to Fh' to the 320 Fh VCO. As a result, output of the phase converter is 40 Fh' ± Δf.
The subconverter is supplied with the Fs signal from the 3.58 MHz VCO and the 40 Fh' ± Δf signal from the phase converter. Therefore, the subconverter outputs Fh' ± Δf of the sum component and Fs – (Fs + 40 Fh' ± Δf) of the difference component.
BPF103 extracts only the Fs + 40 Fh' ± Δf which is the necessary sum component and supplies it to the main converter. Besides this signal, the main converter is supplied with 40 Fh ± Δf from LPF and Fs + 40 Fh' ± Δf from BPF103. Therefore, the main converter outputs Fs + 2 (40 Fh' ± Δf) of the sum component and Fs (color signal) of the difference component.
The comb 1 extracts the Fs (color signal) that is the necessary difference component from the above-mentioned signal.

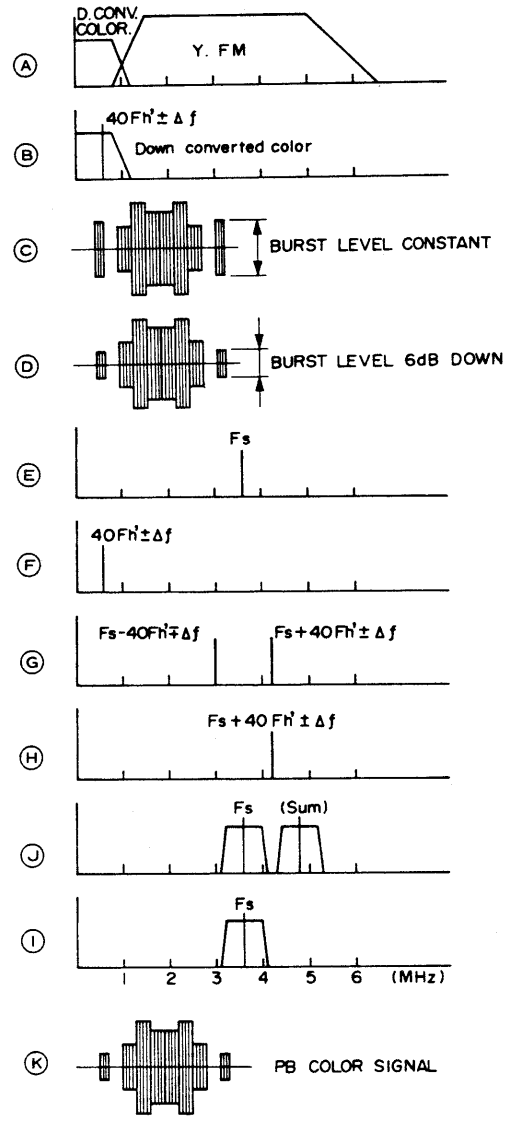


Fig. 4-3-1 PB color signal chart

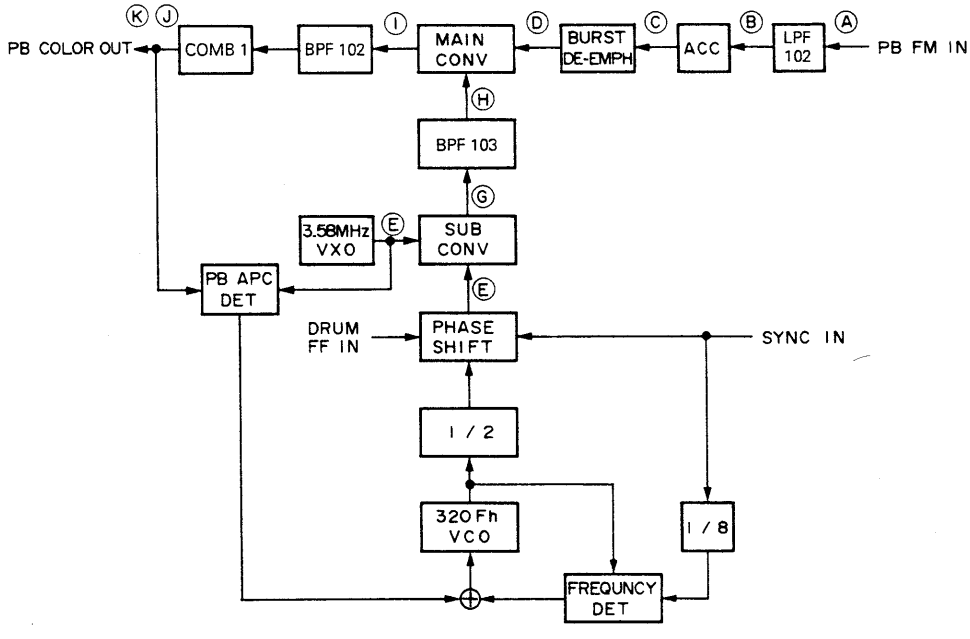


Fig. 4-3-2 Color ACC circuit

4.3.9 Outline of CNR circuit (IC107)

The CNR circuit removes random noise contained in PB color signal and the IC BA7233 is used for this circuit as well as other models. Since this circuit removes noise components by arithmetic processing of PB color signal and the signal 1H before, malfunction may occurs in portions without line correlation and it causes vertical blurring in color. To prevent this problem, non-correlative pulse that is obtained from luminance signal is used to turn off the CNR circuit for the portions without line correlation. Moreover, the CNR circuit is turned off in the Edit mode.

Non-correlative pulse (CNR P) is generated by the YNR block of IC15 and it is output from the pin (34).

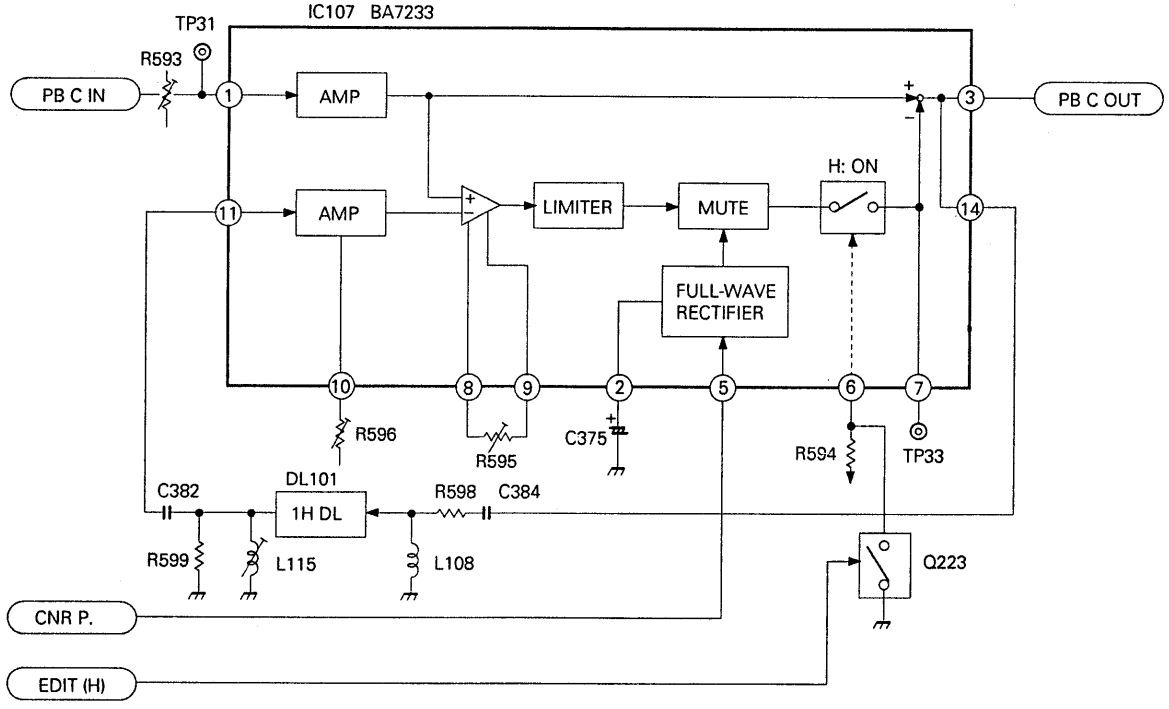


Fig. 4-3-3 CNR circuit

SECTION 5
AUDIO CIRCUIT

● DIFFERENCE BETWEEN BR-S422 AND BR-S411B

Different points	BR-S411B	BR-S422
INPUT SELECT CAMERA MIC input LINE input (VTR)	 –20 dBs –60 dBs –20 dBs +4 dBs	 –20 dBs –60 dBs +4 dBs
VTR MIC input level	–60 dBs (fixed)	–60 dB (Variable by ±10 dB)
CH-1 to CH-2 recording	×	○
Speaker	×	○
REC LEVEL VR Hi-Fi/Norm FIX (Standard setting) function	 Individual setting available ×	 Setting in common ○
LINE output	–6 dBs/–20 dBs, 600 Ω, Balanced	–6 dBs, 1 kΩ, Unbalanced
POWER SAVE operation circuit (GY-X2)	×	○

● GENERAL DESCRIPTION

In regard of the audio circuit of the BR-S422, it is capable of recording 2-channel audio on the normal track and the Hi-Fi track.
The specifications of the input and output circuits are described below.

5.1 INPUT AND OUTPUT SYSTEMS

1. 50-pin multi-connector
   - Balanced input
   - High impedance (50 kohm approx.)
   - Input sensitivity : –20 dBs
2. EXT. MIC terminal
   - Balanced input
   - High impedance
   - Input sensitivity: +4 dBs (10 kΩ)/–60 dBs (3 kΩ)
3. Input attenuator
   - ±10 dB to –60 dB of the EXT. MIC terminal, settable with the internal switch.
4. Limiter characteristic
   - The limiter is activated when the level is +13 dB compared with 0 VU of the reference level, and the limiting range is extendable up to +26 dB.
5. Outline of REC system block diagram
   - Balanced audio signal input through the 50-pin connector is converted into unbalanced audio signal by IC1. In other words, the signal level is expressed against the ground level of the chassis.

   All of input levels are shown in Fig. 5-1-1, which illustrates how respective input levels changes. For example, when input from the 50-pin connector has –20 dBs level, its level is dropped to –30 dBs by the –10 dB amplifier first and then the signal is connected to the switch. At the same time, the signal is transformed from the unbalanced signal to the balanced signal. The amplifier having –10 dB gain is IC1, which has the dynamic range of +38 dB enough for the clipping level at the amplifier's output point as compared with the –20 dB input of the reference level.
6. MIC amplifier circuit
   - In case of mic input, –60 dBs input of the reference level is amplified to –30 dBs by the +30 dB amplifier. The feedback level of this amplifier is variable by additional +12 dB or –10 dB with switch setting, and this variable function is used as the input attenuator. This amplifier is good at the S/N ratio and has 38 dB head room in the gain-up condition up to +10 dB clipping output level.

   The input selector switch (CAM/LINE) in the next stage is switched with the external XLR input by the AUDIO INPUT SELECT switch inside the side panel. In consideration of monaural input from the camera mic, setting of the switch to the CH1 position makes it possible to record camera mic input on the CH2 in addition to the same recording on the CH1.

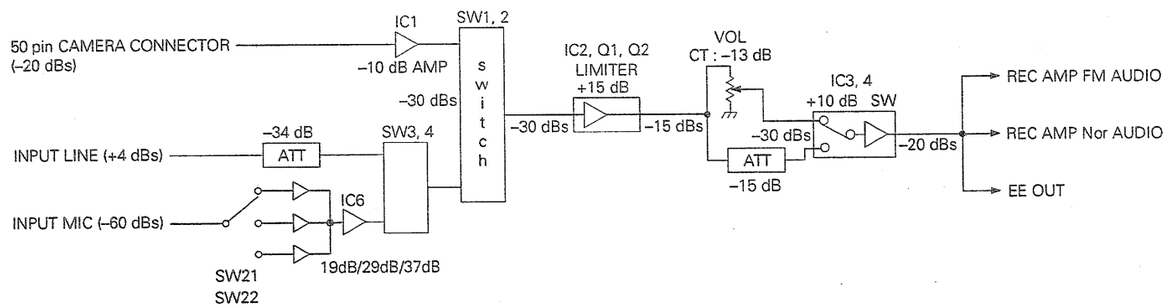
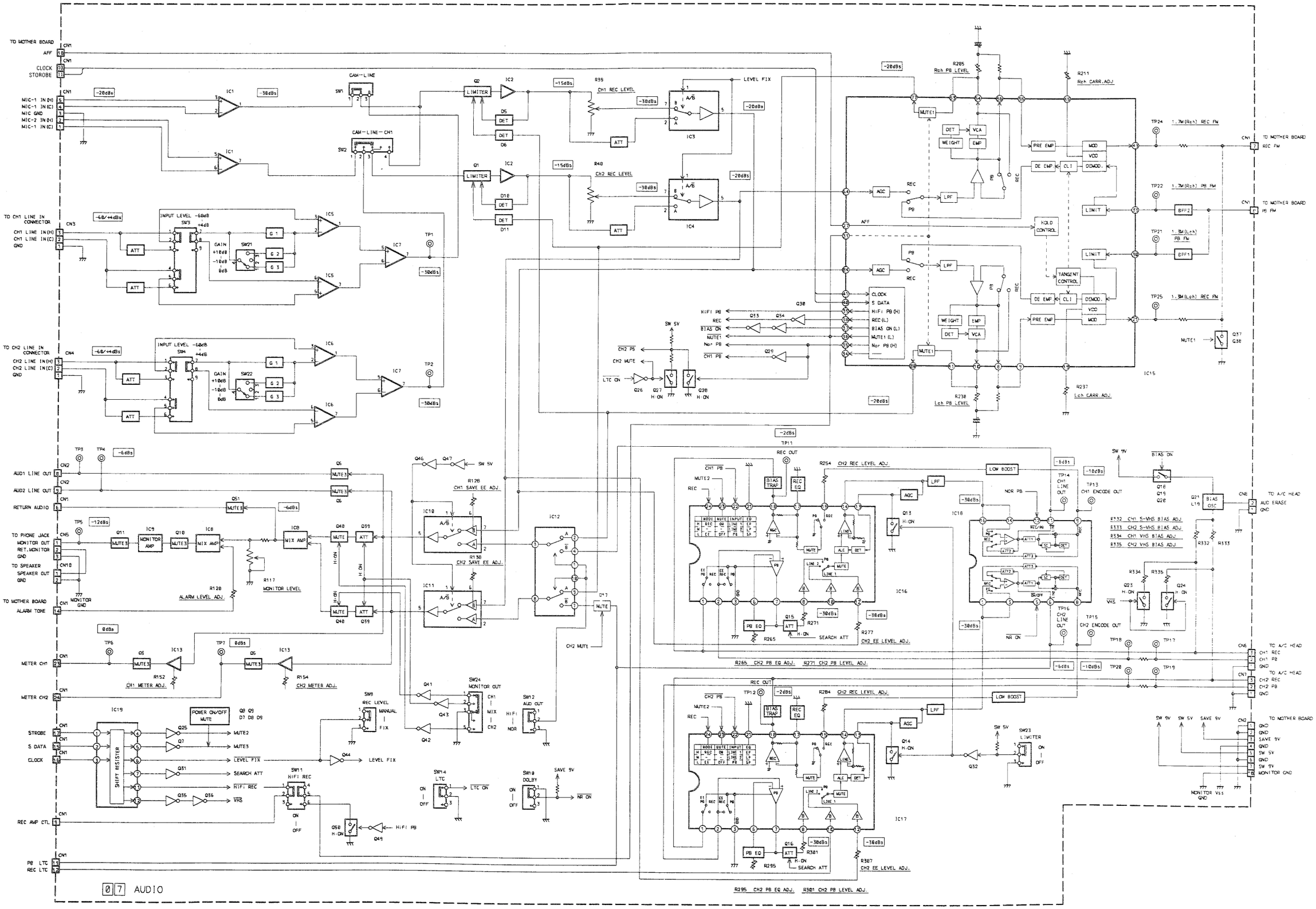


Fig. 5-1-1 Input level diagram

5-1


TO MOTHER BOARD
AFF
CLOCK
STOROBE
MIC-1 IN(H)
MIC-1 IN(C)
MIC GND
MIC-2 IN(H)
MIC-1 IN(C)
CAM-LINE
CAM-LINE-CH1
LIMITER
LEVEL FIX
CH1 REC LEVEL
CH2 REC LEVEL
TO CH1 LINE IN CONNECTOR
CH1 LINE IN(H)
CH1 LINE IN(C)
GND
INPUT LEVEL -60dB +4dB
GAIN +10dB -10dB 0dB
TO CH2 LINE IN CONNECTOR
CH2 LINE IN(H)
CH2 LINE IN(C)
GND
AUD1 LINE OUT
AUD2 LINE OUT
RETURN AUDIO
TO PHONE JACK
MONITOR OUT
RET.MONITOR
GND
TO SPEAKER
SPEAKER OUT
GND
TO MOTHER BOARD
ALARM TONE
MONITOR AMP
MIX AMP
MONITOR LEVEL
ALARM LEVEL ADJ.
METER CH1
METER CH2
CH1 METER ADJ.
CH2 METER ADJ.
STROBE
S.DATA
CLOCK
SHIFT REGISTER
POWER ON/OFF MUTE
MUTE2
MUTE3
LEVEL FIX
SEARCH ATT
HIFI REC
VHS
REC AMP CTL
PB LTC
REC LTC
REC LEVEL
MANUAL
FIX
HIFI REC
DOLBY
SAVE 9V
LTC ON
NR ON
HIFI PB
CH1 SAVE EE ADJ.
CH2 SAVE EE ADJ.
MONITOR OUT
CH1 MIX CH2
HIFI NOR
AUD OUT
CH2 MUTE
SW 5V
SW 9V
REC OUT
CH1 PB
CH2 PB
MUTE1
MUTE2
REC
BIAS TRAP
REC EQ
LPF
AGC
LOW BOOST
NOR PB
R285 Rch PB LEVEL
R211 Rch CARR.ADJ
R238 Lch PB LEVEL
R237 Lch CARR.ADJ
R254 CH2 REC LEVEL ADJ.
R284 CH2 REC LEVEL ADJ.
R265 CH2 PB EQ ADJ.
R271 CH2 PB LEVEL ADJ.
R295 CH2 PB EQ ADJ.
R301 CH2 PB LEVEL ADJ.
R277 CH2 EE LEVEL ADJ.
R307 CH2 EE LEVEL ADJ.
SEARCH ATT
PB EQ
HOLD CONTROL
TANGENT CONTROL
PRE EMP
DE EMP
DEMOD.
MOD
VCO
CLI
LIMIT
BPF2
BPF1
WEIGHT
EMP
DET
VCA
IC15
IC16
IC17
IC18
TP24 1.7M(Rch) REC FM
TP22 1.7M(Rch) PB FM
TP21 1.3M(Lch) PB FM
TP25 1.3M(Lch) REC FM
TO MOTHER BOARD REC FM
TO MOTHER BOARD PB FM
TO A/C HEAD AUC ERASE
TO A/C HEAD CH1 REC CH1 PB GND
TO A/C HEAD CH2 REC CH2 PB GND
TO MOTHER BOARD SAVE 9V GND SW 5V GND SW 9V MONITOR GND
R332 CH1 S-VHS BIAS ADJ.
R333 CH2 S-VHS BIAS ADJ.
R334 CH1 VHS BIAS ADJ.
R335 CH2 VHS BIAS ADJ.
BIAS OSC
BIAS ON
CH1 ENCODE OUT
CH2 ENCODE OUT
CH1 LINE OUT
CH2 LINE OUT
07 AUDIO

7. Limiter amplifier circuit

- The limiter amplifier (IC2) that is newly employed in the BR-S422 functions to record over-level input without distortion, therefore, it is activated only when input has excessively over-level and has not gain adjustment function for low level input. The standard output level of this limiter amplifier is –15 dBs, and it automatically controls output level not to exceed the standard level and + 6 dB at maximum.

IC2 is an operational amplifier whose gain is determined by R14 and R13. The gain G is generally expressed by the following equation.

$G = 1 + (R13/R14) = 1 + 220\ k\Omega/47\ k\Omega = 5.68$ times
$= 15$ dB.

However, there is the attenuator circuit composed of R11 and R32 in the input circuit, therefore, the circuit composed of Q2 FET and R25 connected in parallel is connected with R32 in series. As a result, the attenuator continuously varies attenuation level up to –26 dB according to the resistance of Q2 when Q2's level is in the range between –0.1 dB and the full capacity.

When a DC voltage which is higher than the specific DC voltage (4 V) determined by R33 and R34 and rectified by D6 is applied to Q2, resistance between the drain and the source declines and the attenuator starts operation to decrease the input level of the IC (see Fig. 5-1-2).

In the same manner, DC voltage rectified by D10 is impressed to Q2 in order to prevent over-modulation by monitoring the output level that is logarithmically compressed to 6 dB at frequency modulation.

This loop circuit has the time constant determined by C16 and R19,R20 but the time constant has been changed in the halfway of the production of this model and now the attack time and the recover time are 0.85 msec and 4 sec respectively, which are convenient for smooth operation of the VTR.

Moreover, output of D14 is supplied to the limiter circuit, too, and this signal is added with muting pulse that is generated when Q8 and Q9 get SW 9V and SAVE 9V pulses to rise for the purpose of preventing recording signal from getting noise mixing.

8. REC level adjuster circuit

- Output of IC2 is attenuated by –15 dB by R35 and R36 when the REC LEVEL switch inside the side panel is set to FIX. When this switch is set to the MANUAL, recording level can be adjusted by the AUDIO REC LEVEL VR on the side panel.

The setting of the REC LEVEL switch to the FIX position is useful in emergency since the level is nearly equal to the level when the volume is set to the mid point.

IC3 which incorporates an analog switch capable of selecting adjusting signal inside functions to control recording level so that it inputs signal supplied to pin ⑦ from between two signals supplied to pins ⑦ and ② when the pin ① has "H" level. The "L" level of pin ① is not 0 V but about 4.5 V equivalent to 1/2 Vcc for the reason of the linarity of the amplifier, and "L" level is supplied by R167 connected with the collector of the transistor switch Q44.

The signal whose level is adjusted as mentioned above is supplied to the normal recording amp (IC16) and the Hi-Fi recording amp (IC15). IC10 adjusts the signal level to be the reference PB level (–6 dBs) by R128, and the signal is output as EE output signal from the AUDIO-1 terminal.

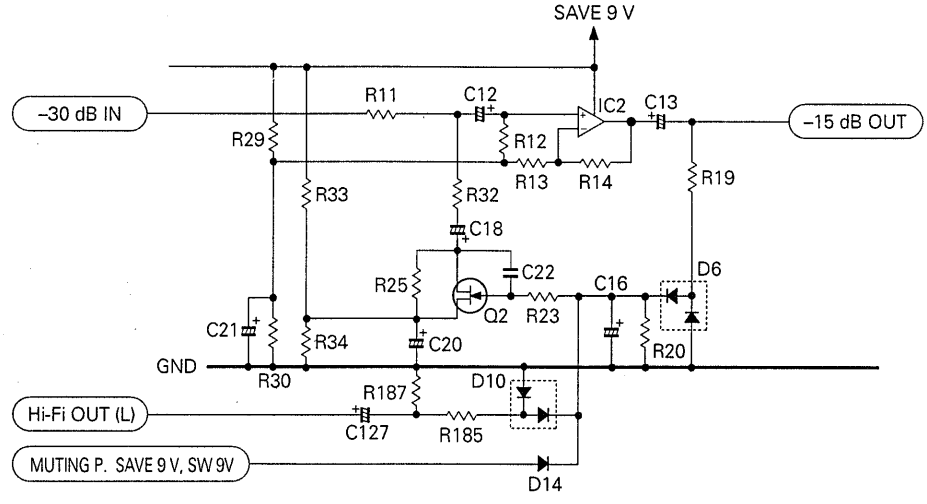


Fig. 5-1-2 Limiter circuit (L-ch)

9. Change of line level (from +4 dBs to –20 dBs)

- The XLR input connector is switchable for MIC input or LINE input by switching the –60 dBs/+4 dBs sensitivity selector switch. When recording mic signal input through the LINE IN connector at a wedding ceremony/reception, for example, it is hard to obtain sufficient level for recording with the setting to +4 dBs since the standard level is –20 dBs in most cases. On the other hand, if 10 dB attenuator is used for the –60 dBs setting, the sensitivity is –50 dBs that is still too high and useless for actual recording. Therefore, it may be necessary to change the sensitivity to –20 dB with the +4 dB setting. In this case, it is suggested to change the attenuator level to –10 dB from the present –34 dB. To obtain the required sensitivity, replace R62 (180 Ω) that determines the attenuation level with a 3.3 kΩ resistor.

10. Monitor output circuit

- IC12 of the analog switch selects monitor signal, and PB audio output can be selected with the MONITOR OUT switch on the operation panel. The selection function of this IC is activated only in the playback mode.

  In the playback mode, CH1 and CH2 signals are supplied to pin ① by IC10 and IC11 respectively and pin ② is selected by the control signals yielded from the SW9V signal whose level is "H" in this mode by Q46 and Q47 respectively to output playback signal.

  Signal output from pin ⑤ is supplied through the muting circuit of Q6 and the MOTHER board to the RCA pin terminal on the CONNECTOR board, and it is output from the connector. On the other hand, the signal from pin ⑤ is also supplied to IC13 and IC18 as the meter indication signal and the output signal for the headphone.

  Q39 and Q40 function as the switch circuit. When Q3 is off in the MIX mode selected by the MONITOR OUT switch on the subpanel, mixture of CH1 and CH2 signals is output as the headphone signal. When Q40 is turned off by the switch, signal on one channel is selected to output.

  Alarm signal output from the headphone is generated by mixing the alarm tone signal that is output from IC17 of the CPU in emergency and at the tape end after level setting by R120 of the MONITOR LEVEL control.

  Q10 and Q11 suppress generation of phut noise generated when the mode is shifted to the playback.

5.2 Hi-Fi AUDIO RECORDING SYSTEM

IC15 is the Hi-Fi audio recording amp. whose pin 84 is used for signal input and its reference input level is –20 dBs. This IC is equipped with an internal AGC gain amp. but it has no gain as 0 dB since pin ③ is of 0 Ω.

After mode is shifted from REC to PB, the LPF limits frequencies higher than 20 kHz and drives the PNR (Peak Noise Reduction) circuit. Regarding this circuit brief explanation appears in the following since there are detailed explanations in many instructions of other models.

In the Hi-Fi recording system of the VHS format, the frequencies of two carriers of CH1 (1.3 MHz) and CH2 (1.7 MHz) are modulated in the range of ±50 kHz, and the FM signals are recorded on the video track by the Hi-Fi REC head.

To obtain sufficient dynamic range with a low f/c ratio (ratio between frequency deviation and carrier frequency), 2:1 logarithmic compression is applied in the periods of 240 µsec and 24 µsec (663 Hz to 6631 Hz) for bottom-up recording at the level of 6 dB/oct. Those operations are performed by the VCA, PEAK DET and WEIGHTING circuit connected with pins ⑧, ⑨ and ⑩ respectively.

The pre-emphasis circuit which is installed to prevent deterioration in S/N ratio caused by so-called triangular noise that frequently occurs in the FM recording system emphasize high frequencies of 56 µsec and 20 µsec (2842 Hz to 7958 Hz) by the level of 6 dB/oct.

The VCO circuit applies frequency modulation to carriers, and there is a limiter circuit used for preventing over-modulation not to exceed the utmostmodulation limit of ±150 kHz. The LPF which is installed in the previous stage of pin ㉑ to output signal prevents video signal from getting undesirable influence of higher harmonic distortion.

IC15 has the command demodulation circuit, which converts serial command from the syscon into parallel data together with IC19 to control the audio circuit.

5.3 NORMAL AUDIO SYSTEM

5.3.1 IC16, IC17 (LA7285M)

The LA7285M, the main IC for normal audio, incorporates the LINE amp, REC amp, PB amp and the limiter circuit inside.

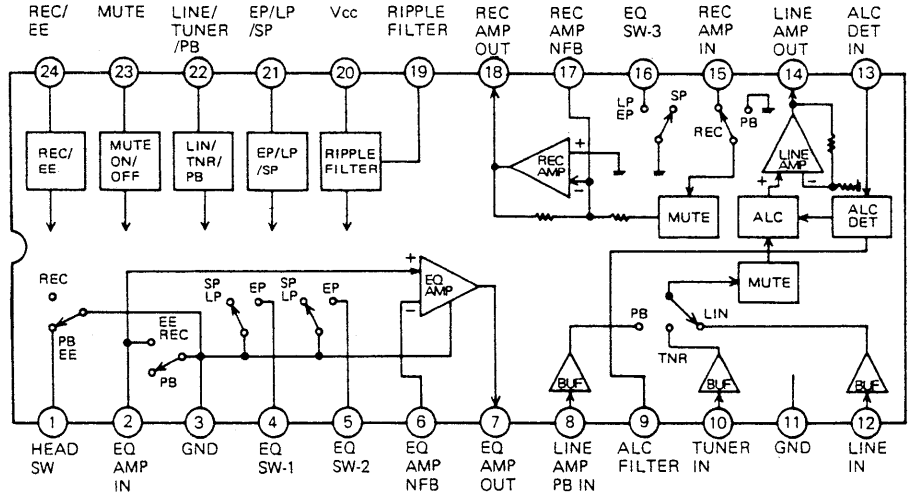


Fig. 5-3-1 Block diagram

- Pin functions

Pin No.	Name	Function
1	HEAD SW 1	ON : EE and PB modes, OFF : REC modes
2	EQ AMP INPUT and HEAD SW 2	PB signal input from audio head ON : EE and REC modes, OFF : PB mode
3	GND	Ground for exclusive use of head switch of pin ①, EQ amp. and PB EP switch
4	EP SW 1	Not used
5	EQ SW 2	Not used
6	EQ AMP NFB	To apply negative feedback for demonstrating equalizer characteristic
7	EQ AMP OUTPUT	
8	LINE AMP PB INPUT	PB signal input from EQ amp.
9	ALC FILTER	Detection and setting of attack time and recovery time according to the time constant of CR.
10	TUNER INPUT	CH2 for input of time code signal (LTC)
11	GND	Ground for circuits and blocks except head switch and EQ amp circuit
12	LINE INPUT	EE, REC signal input
13	ALC DETECTION INPUT	ALC level is determined by atten uation by R255, R256 (CH1) and R285, R286 (CH2).
14	LINE AMP OUTPUT	
15	REC AMP INPUT	Recording current is set by R254 (CH1) and R284 (CH2). REC amp. is inversional amp.
16	LP SW	Not used
17	REC AMP NFB	To boost high frequency response depending on L, C, R connected.
18	REC AMP OUTPUT	
19	RIPPLE FILTER	
20	POWER SUPPLY (Vcc)	To remove ripple with capacitor
21	EP/LP/SP CONTROL	H: EP, M: LP, L: SP
22	LINE TUNER PB CONTROL	H: LINE, M: TUNER, L: PB
23	MUTE CONTROL	H: MUTE ON, M: —, L: MUTE OFF
24	REC/EE CONTROL	H: EE, M: —, L: REC

Table 5-3-1

5.3.2 IC18 (CXA1102M)

IC18 is the 2-channel Dolby B type noise reduction circuit. Its encoding characteristic is shown in Fig. 5-3-2.

Pin ⑤ switches NR on/off.
"H" : NR OFF, "L" : NR ON

Pin ⑫ switches REC/PB.
"H" : PB (decoding), "L" : REC (encoding)

5.3.3 REC amp circuit

The REC amp circuit includes the low boost circuit composed of C208, C209, C210, R259, R260 and R261, and the REC amp. of IC16 to compensate high component loss in recording and playback. This circuit has a high boost equalizing characteristic which is shown in Fig. 5-3-3.

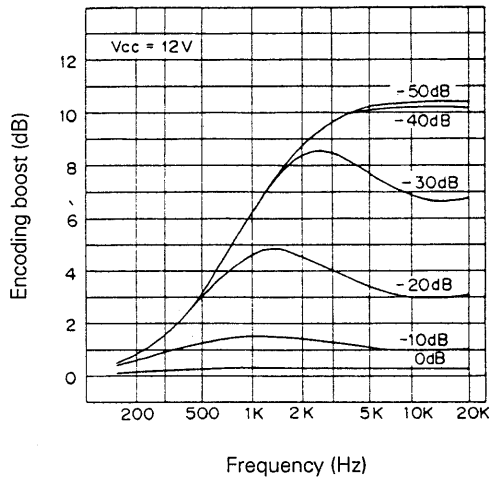


Fig. 5-3-2 Encoding characteristic

5.3.4 PB equalizer

Normal audio output from the A/C head is supplied to IC16 through pin ② (L-ch) and amplified by the PB amp inside the IC. This IC applies negative feedback to the signal so as to function as the PB equalizer amp. The frequency characteristic of this PB equalizer amp is shown in Fig. 5-3-4.
Signal input through pin ⑦ is supplied to R271 to adjust the PB level and again input from pin ⑧. After that, signal flow is the same as in recording.

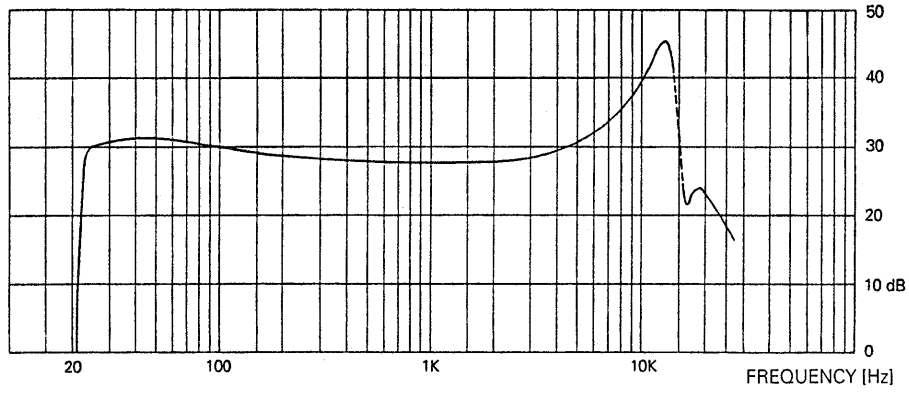


Fig. 5-3-3 Recording frequency response

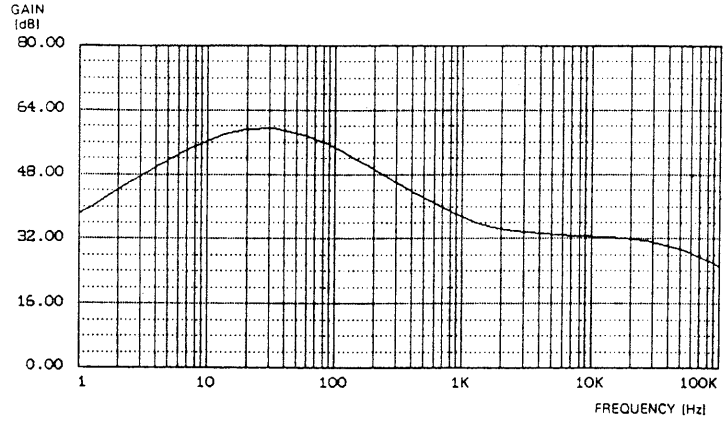


Fig. 5-3-4 Frequency response of PB EQ amp.

SECTION 6
MECHANISM OPERATION

6.1 FUNCTION OF MOTORS

6.1.1 Drum motor

The drum motor composed of a stator and rotor inside the lower drum drives the upper drum to which video heads are attached.

6.1.2 Capstan motor

The capstan motor forwards and rewinds the tape by rotating in the normal and reverse directions.

1. By normal rotation of the capstan motor the take-up gear comes to the TU (take-up) side.
   In the PB (playback) mode, rotation of the capstan motor is transmitted to the take-up reel disk via the clutch mechanism.
2. By reverse rotation of the capstan motor the take-up gear comes to the SUP (supply) side.
   In the REV (Reverse; Search REW) mode, the clutch mechanism transmits rotation of the capstan motor to the supply reel disk.
3. By normal rotation of the capstan motor the take-up idler which is in contact with the pulley gear comes to the TU side.
   In the FF (Fast Forward) mode, rotation of the capstan motor is directly transmitted to the take-up reel disk. (See Fig. 6-1-2.)
4. When the capstan motor rotates reversely, the take-up idler comes to the SUP side.
   In the REW (Rewind) mode, rotation of the capstan motor is directly transmitted to the supply reel disk.

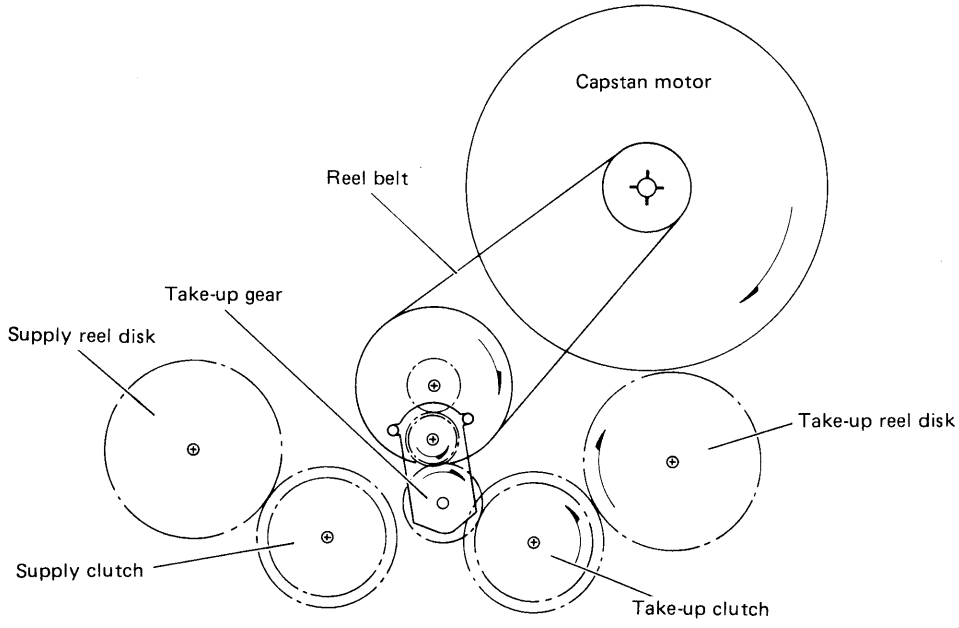


Fig. 6-1-1 Capstan motor's function (in PB mode)

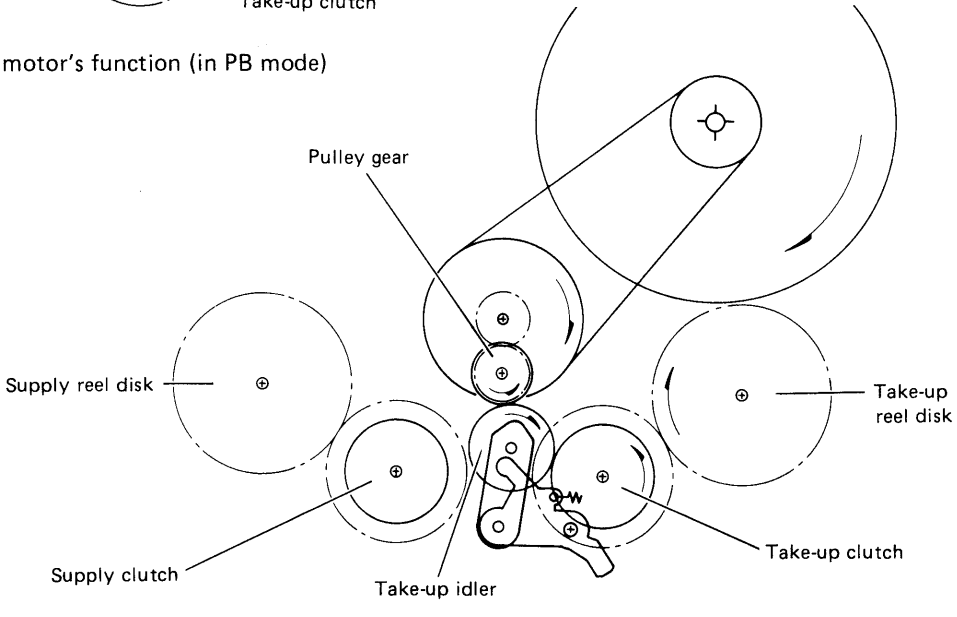


Fig. 6-1-2 Capstan motor's function (in FF mode)

6.1.3 Mode control motor

The mode control motor rotates in the normal or reverse direction to move the control cam which shifts component parts for the selected mode.

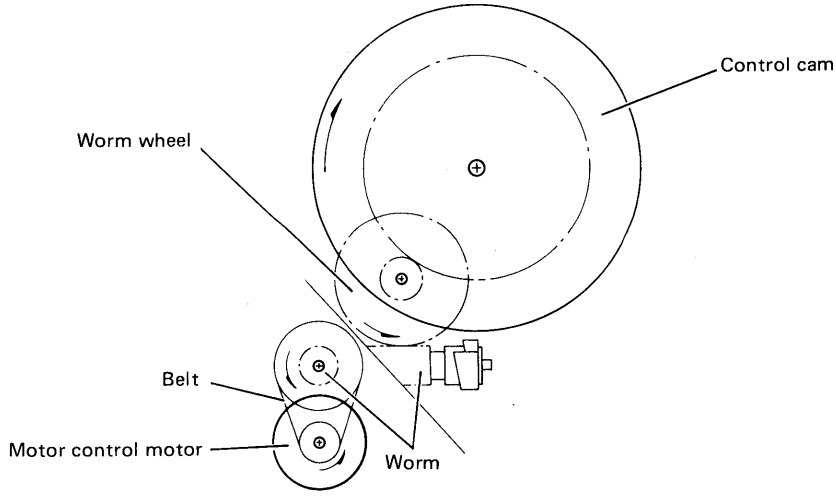


Fig. 6-1-3 Mode control motor's function (in Loading direction)

6.2 MODE SHIFT

The control cam changes its position appropriately for shifting the component parts so that they works to meet the selected mode.

Symbol No.	Mode	Details of Mode
1	EJECT	Ejection (to take out cassette)
2	FF/REW	FF (Fast Forward), REW (Rewind), Short FF
3	STOP	Stop, Short REW Loading, Unloading
4	PLAYBACK	Playback, Still, Shuttle Search (+), REC (Recording), INSERT (Insertion), After-recording
5	BACK SPACE	Back spacing
6	PAUSE	Pause
7	REVERSE	REV (Reverse), Shuttle Search (–), Preroll

——→ : in the Loading direction
– – – – – – → : in the Unloading direction

Table 6-2-1 Mode shift

6.2.1 **Stop mode** (Symbol No. 3)

1. In this mode, the main brake is in close contact with the clutch to prevent the tape from slackening in the cassette.
2. The take-up idler is fixed at the neutral position by function of the cam (3).

   Cam (3) → Slide plate → Relay lever → TU idler ┐
   ┌→ Control plate

3. Both the FF brake and REW brake are in contact with the reel disk.
4. The search brake is off the reel disk by function of the cam (1). (Fig. 6-2-2)
5. The pinch roller is positioned considerably apart from the capstan by function of the cam (2). (Fig. 6-2-3)

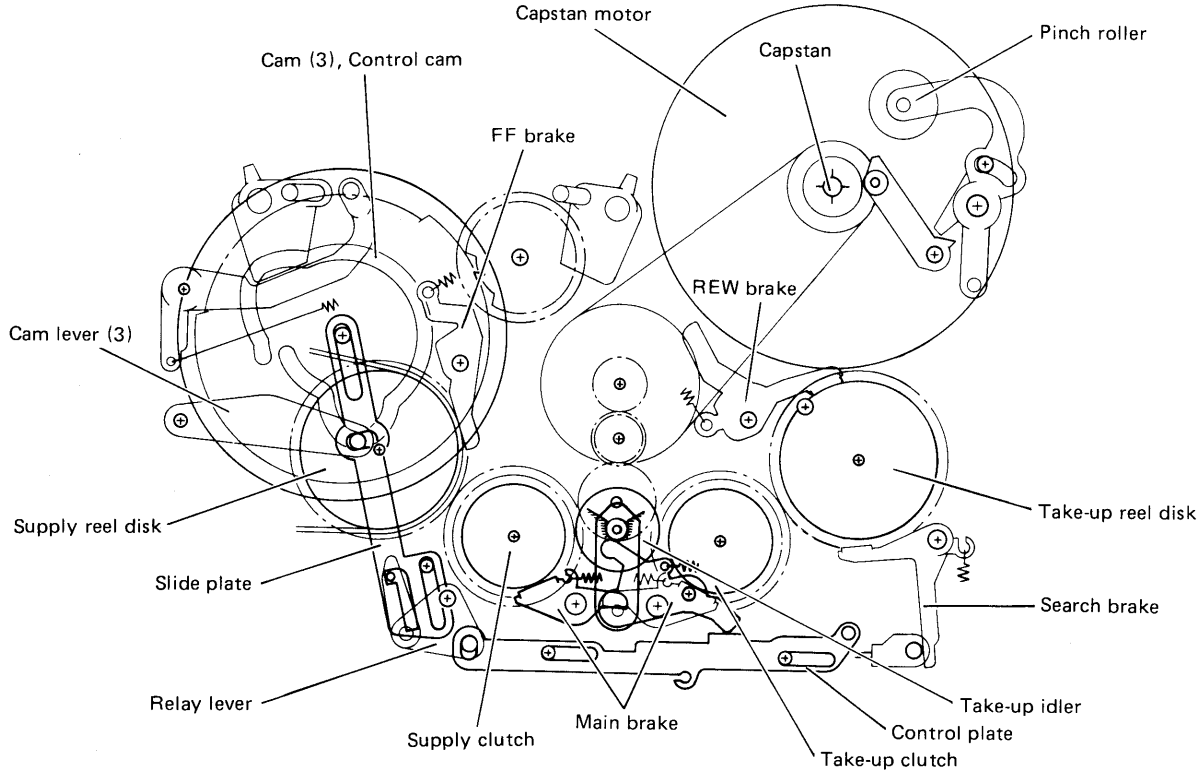


Fig. 6-2-1 Stop mode

6.2.2 **Loading motion** (Symbol Nos. 3 to 4)

1. Not to disturb tape travel from the cassette the main brake is off the clutch by function of the cam (3). (Fig. 6-2-6)
2. As the FF brake and REW brake are in contact with the reel disk, tape is prevented from slackening caused by inertia.
3. The search brake is off the reel disk by function of the cam (1).

   Cam (1) → Cam lever (2) → Rod (1) → Rod (2) →
   → Search brake

4. The pinch roller is in contact with the capstan by function of the cam (2). (Fig. 6-2-3)
5. The mode control motor normally rotates to drive the loading ring in order to pull tape out of the cassette.

   Mode control motor → Worm → Worm wheel →
   → Control cam → Loading gear → Supply loading ring → Connect gear → Take-up loading ring

6. The take-up gear lays a load on the take-up clutch by gearing into it so that tape is mainly pulled out of the supply side.

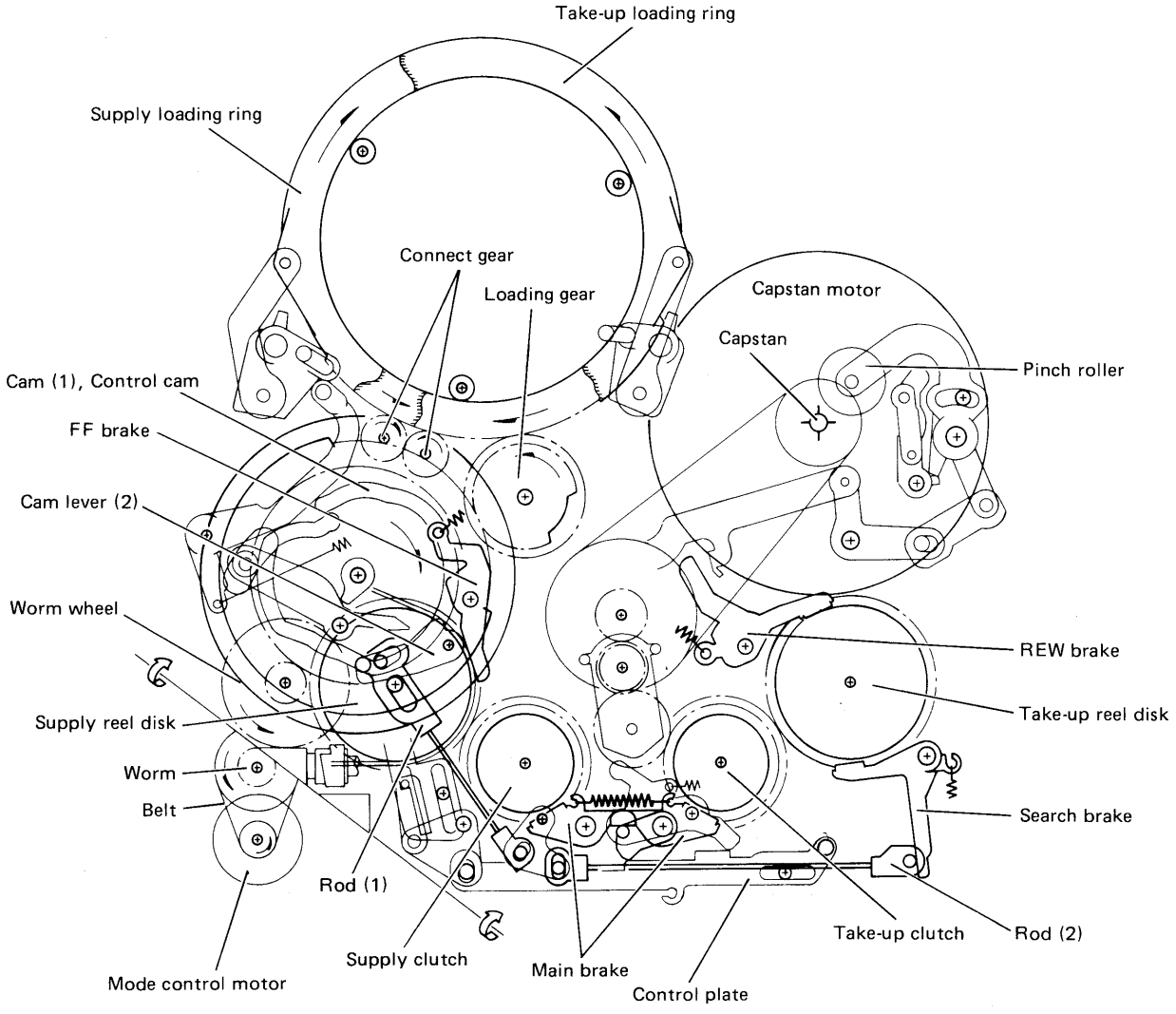


Fig. 6-2-2 Loading motion

6.2.3 **Playback mode** (Symbol No. 4)

1. The main brake is off the clutch by function of the cam (3) not to disturb tape in travel. (Fig. 6-2-6)
2. Both the FF and REW brakes are off the reel disk by function of the cam (2).

   Cam (2) → Cam lever (1) → Relay arm → PR plate ┐
   ┌→ FF brake
   └→ REW brake

3. The search brake is off the reel disk by function of the cam (1). (Fig. 6-2-2)
4. By function of the cam (2) the pinch roller is in contact with the capstan for tape travel.

   Cam (2) → Cam lever (1) → Relay arm → PR plate ┐
   └→ Toggle arm → Pinch roller

5. The capstan motor is rotating to forward and rewind tape. (Fig. 6-1-2)
6. Together with the tension band the tension pole controls back-tension applying it to tape.

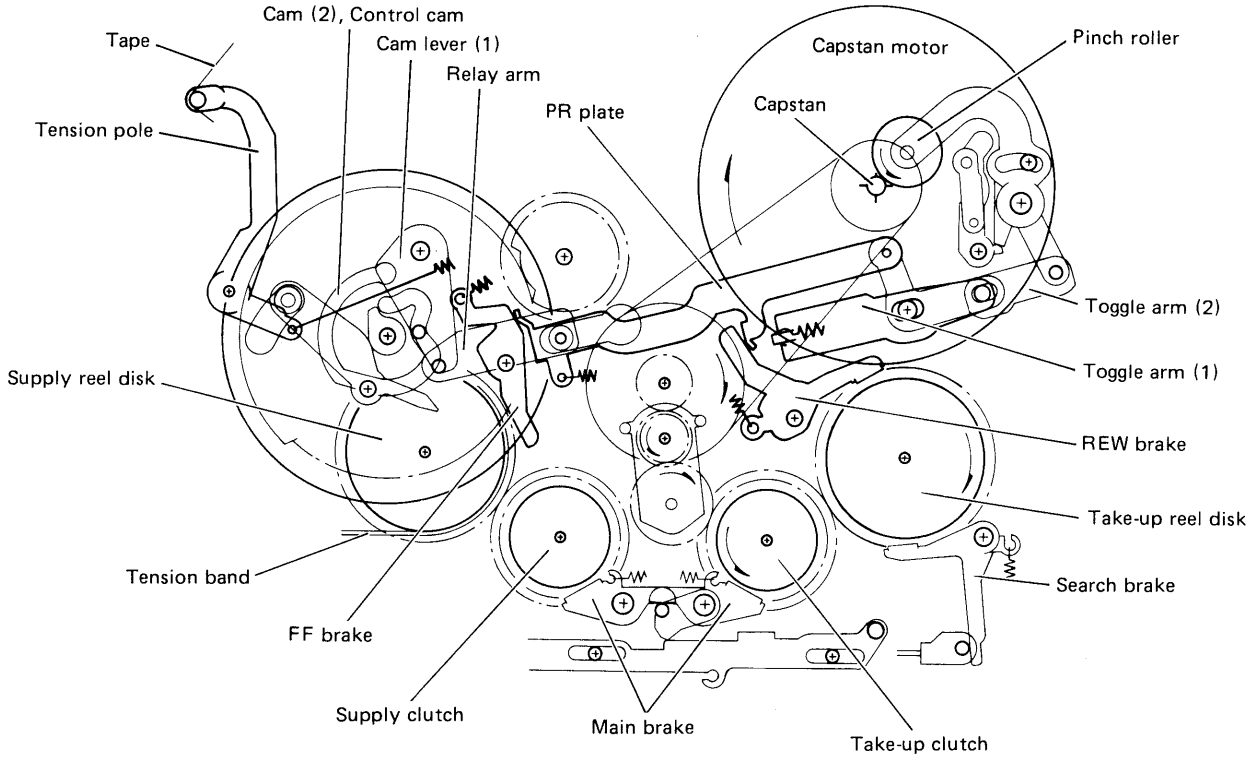


Fig. 6-2-3 Playback mode

6.2.4 **Pause mode** (Symbol No. 6)

1. The main brake is in close contact with the clutch in order to prevent tape from slackening in the cassette.
2. Both FF and REW brakes are in contact with the reel disk.
3. The search brake slightly contacts the reel disk.
4. The tension pole decreases tension to tape by function of the cam (1).

   Cam (1) → Cam lever (2) → Rod (1) → Cancel lever ┐
   └→ Tension pole

5. Capstan motor is stopping.
6. The pinch roller is slightly off the capstan by function of the cam (2). (Fig. 6-2-3)

6.2.5 **Back-space mode** (Symbol No. 5)

1. Motion in this mode is the same as that in the playback mode except the following items (2) through (4). (Fig. 6-2-3)
2. The search brake slightly contacts the reel disk. (Fig. 6-2-4)
3. The tension pole decreases tension to tape by function of the cam (1). (Fig. 6-2-4)
4. The capstan motor rotates to turn tape travel backwards and rewind the tape by the supply reel disk.

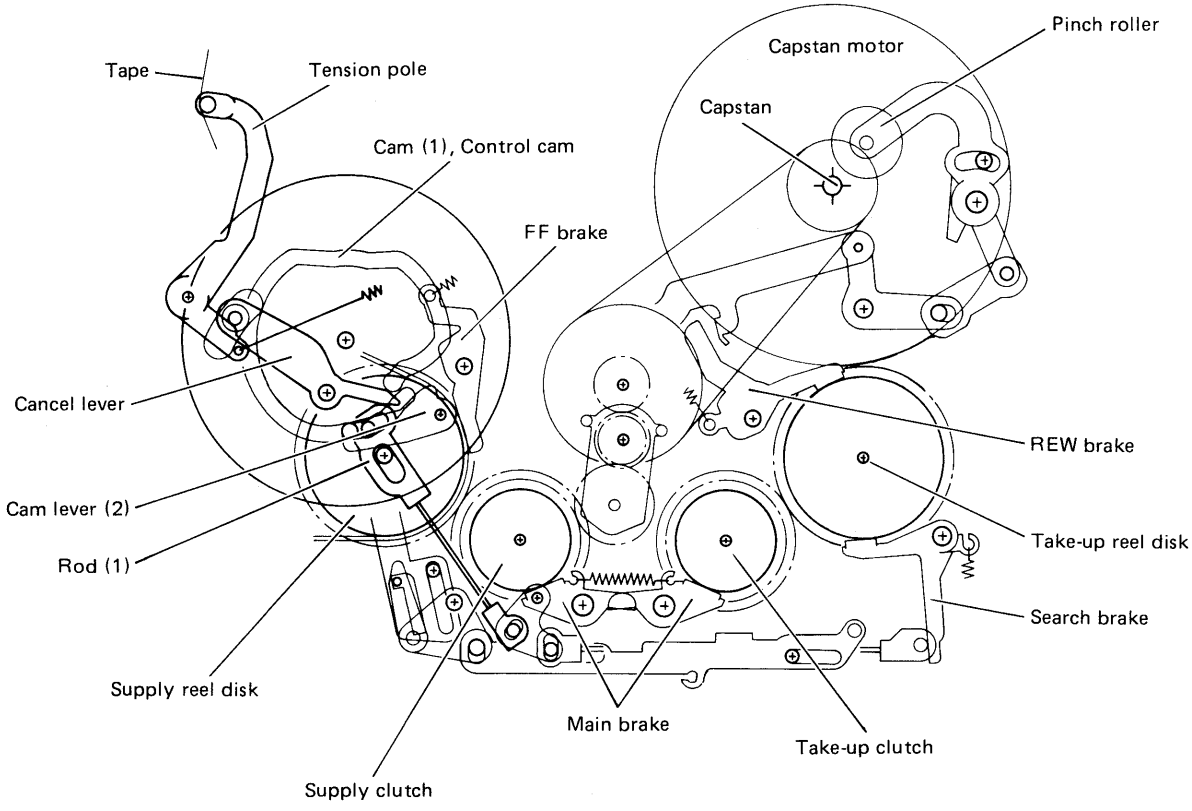


Fig. 6-2-4 Pause mode

6.2.6 **Reverse mode** (Symbol No. 7)

1. The main brake is off the clutch by function of the cam (3). (Fig. 6-2-6)
2. Both the FF and REW brakes are off the reel disk by function of the cam (2). (Fig. 6-2-3)
3. The search brake slightly contacts the reel disk to prevent tape from slackening resulting from inertia.
4. The capstan motor rotates to transport and rewind tape. (Fig. 6-1-2)
5. The tension pole releases tape from back-tension by function of the cam (1).
6. The pinch roller is in contact with the capstan by function of the cam (2) in order to transport tape. (Fig. 6-2-3)

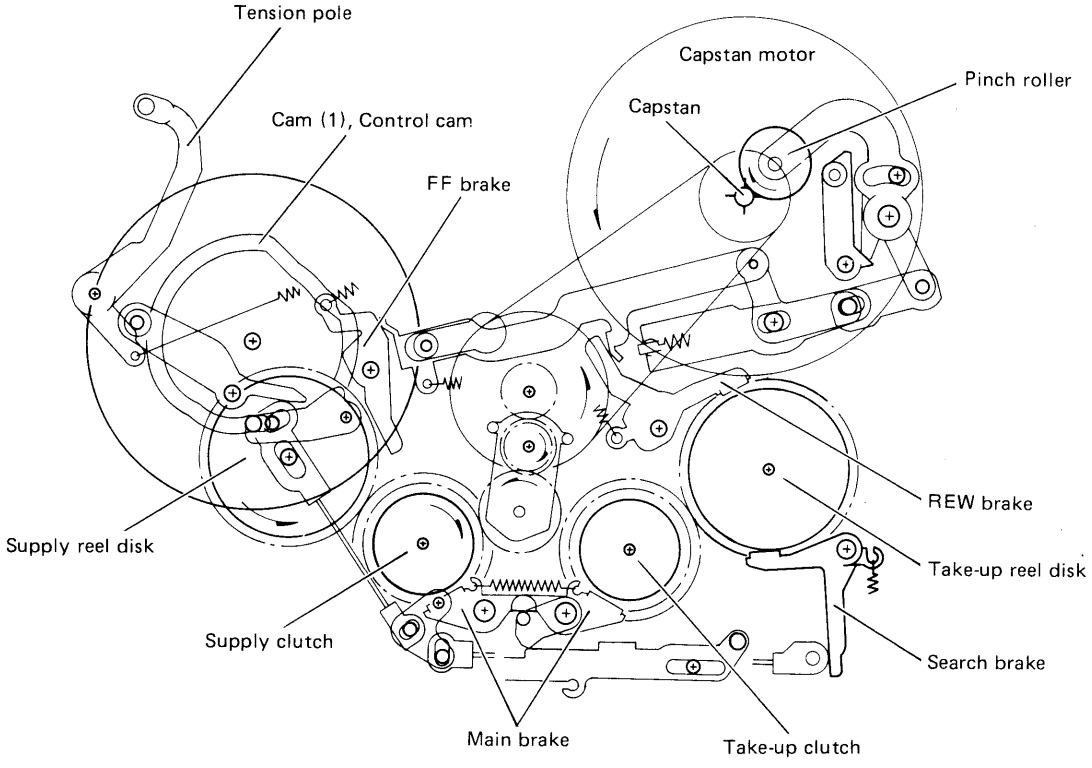


Fig. 6-2-5 Reverse mode

6.2.7 **FF/REW mode** (Symbol No. 2)

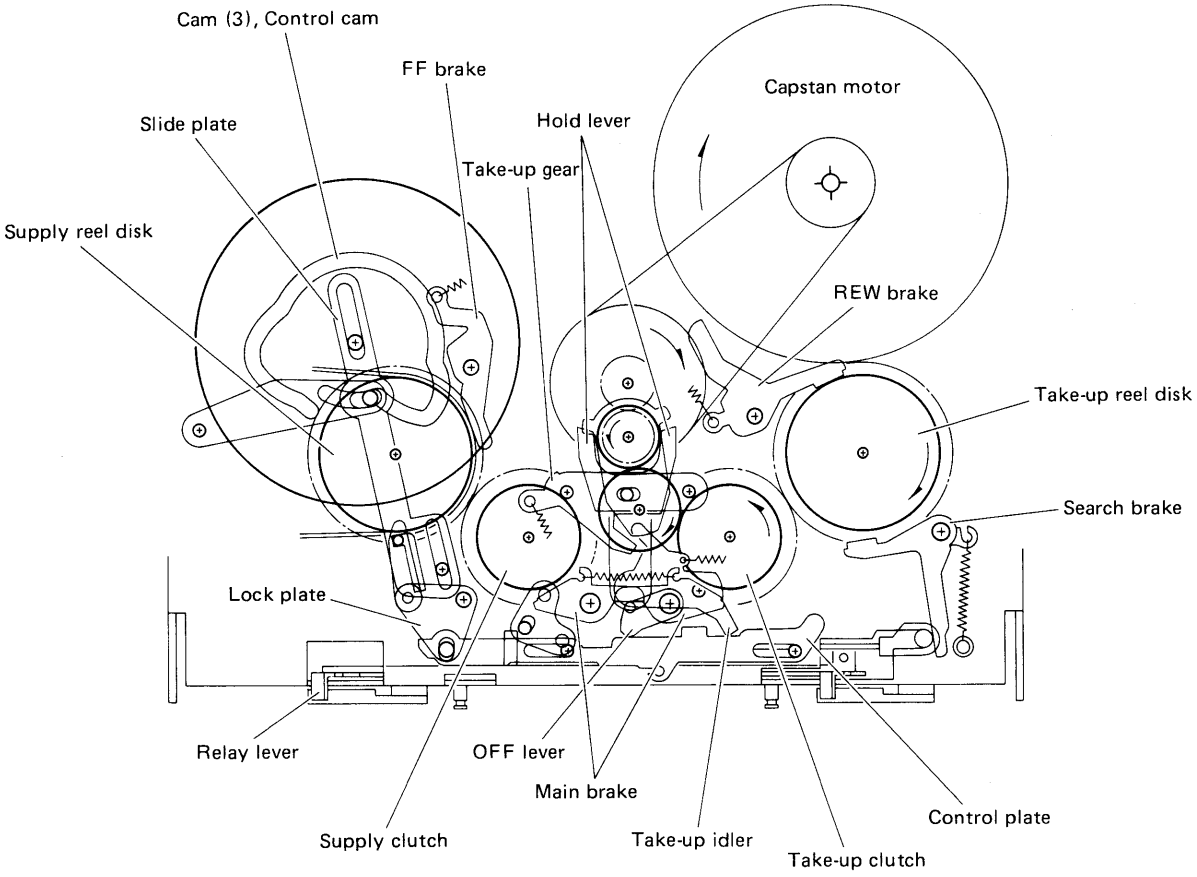
1. The main brake is off the clutch by function of the cam (3).

   Cam (3) → Slide plate → Relay lever → Control plate
   → Off lever → Main brake

2. The TU gear is fixed at the neutral position by the hold bar according to function of the cam (3).

   Cam (3) → Slide plate → Relay lever → Control plate
   → TU idler → Hold lever

3. Both the FF and REW brakes are in contact with the reel disk to prevent tape from inertia resulting from inertia.
4. The search brake is off the reel disk by function of the cam (1). (Fig. 6-2-2)
5. The rod (2) is off the lock plate.
6. The capstan motor rotates to transport tape from the SUP side to the TU reel in the FF mode, for example. (Fig. 6-2-1)
7. The housing arm stud is locked by the lock plate.



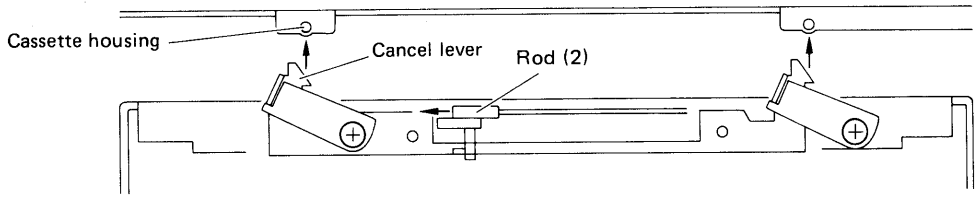


Fig. 6-2-6 FF mode

8. The cam brake is in contact with the brake cam by function of the cam (3).

Cam (3) → Slide plate → Relay lever → Cam brake

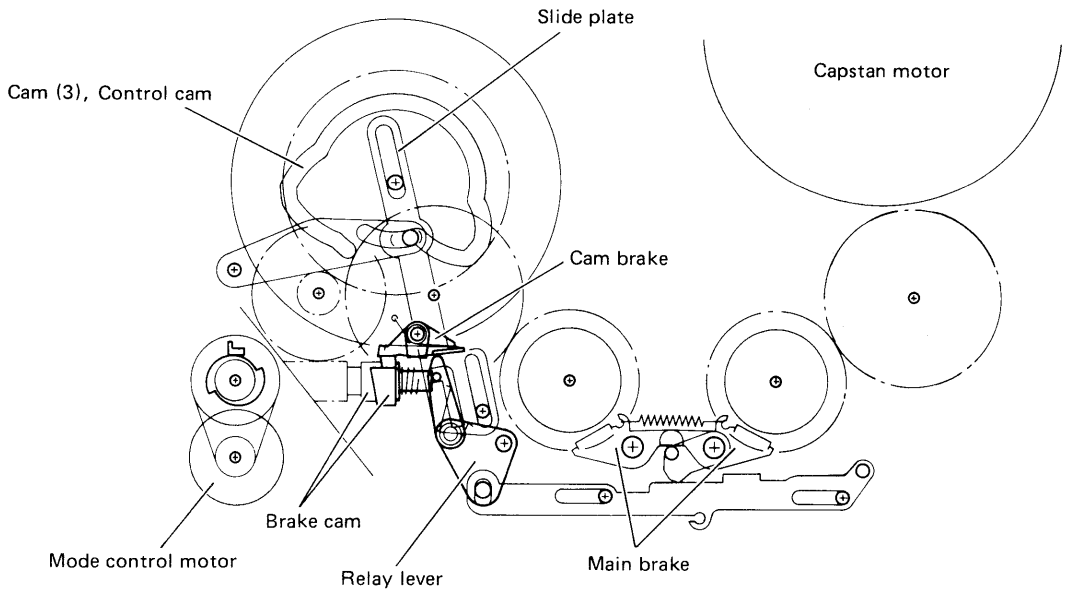
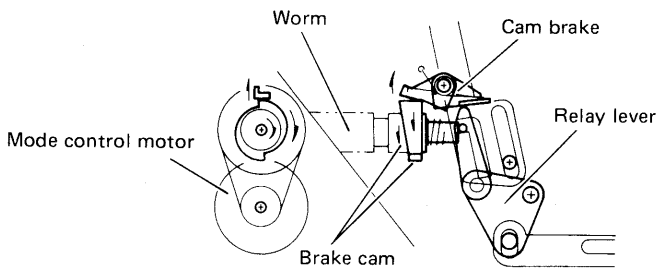


Fig. 6-2-7 FF/REW mode

9. When the mode is changed from the FF/REW to the EJECT, the mode control motor reversely rotates. As a result, the brake cam rotates pushing the cam brake aside. (Reverse rotation: in clockwise direction in the figure)



10. On the other hand, when the mode is changed from this to the STOP, the mode control motor normally rotates and the cam brake stops rotation of the brake cam, which therefore pushes the kick lever to release the relay lever from the slide plate. At this time, the main brake and the capstan brake immediately start in operation.

Mode control motor → Worm → Brake cam
↑
→ Kick lever → Relay lever → Cam brake
→ Control plate
→ Main brake
→ Capstan brake

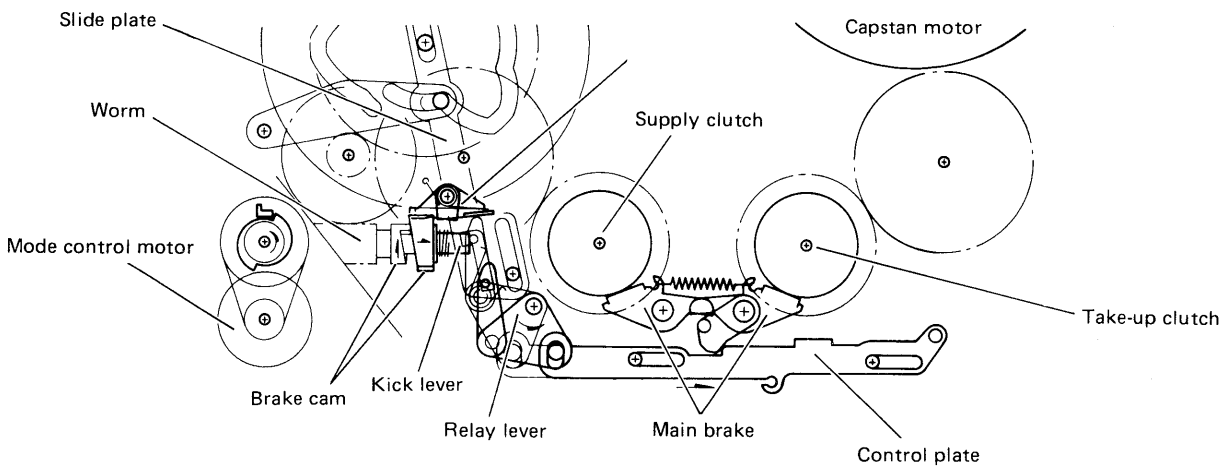


Fig. 6-2-8 Cam brake motion

6.2.8 **Eject mode** (Symbol No. 1)

1. The rod (2) pushes the lock plate by function of the cam (1) in order to release the housing arm stud from the lock plate.

   Cam (1) → Cam lever (2) → Rod (1) → Rod (2) ┐
   └→ Lock plate

2. The main brake is off the clutch by function of the cam (3). (Fig. 6-2-6)
3. Both the FF and REW brakes are in contact with the reel disk.
4. The search brake is in contact with the reel disk.

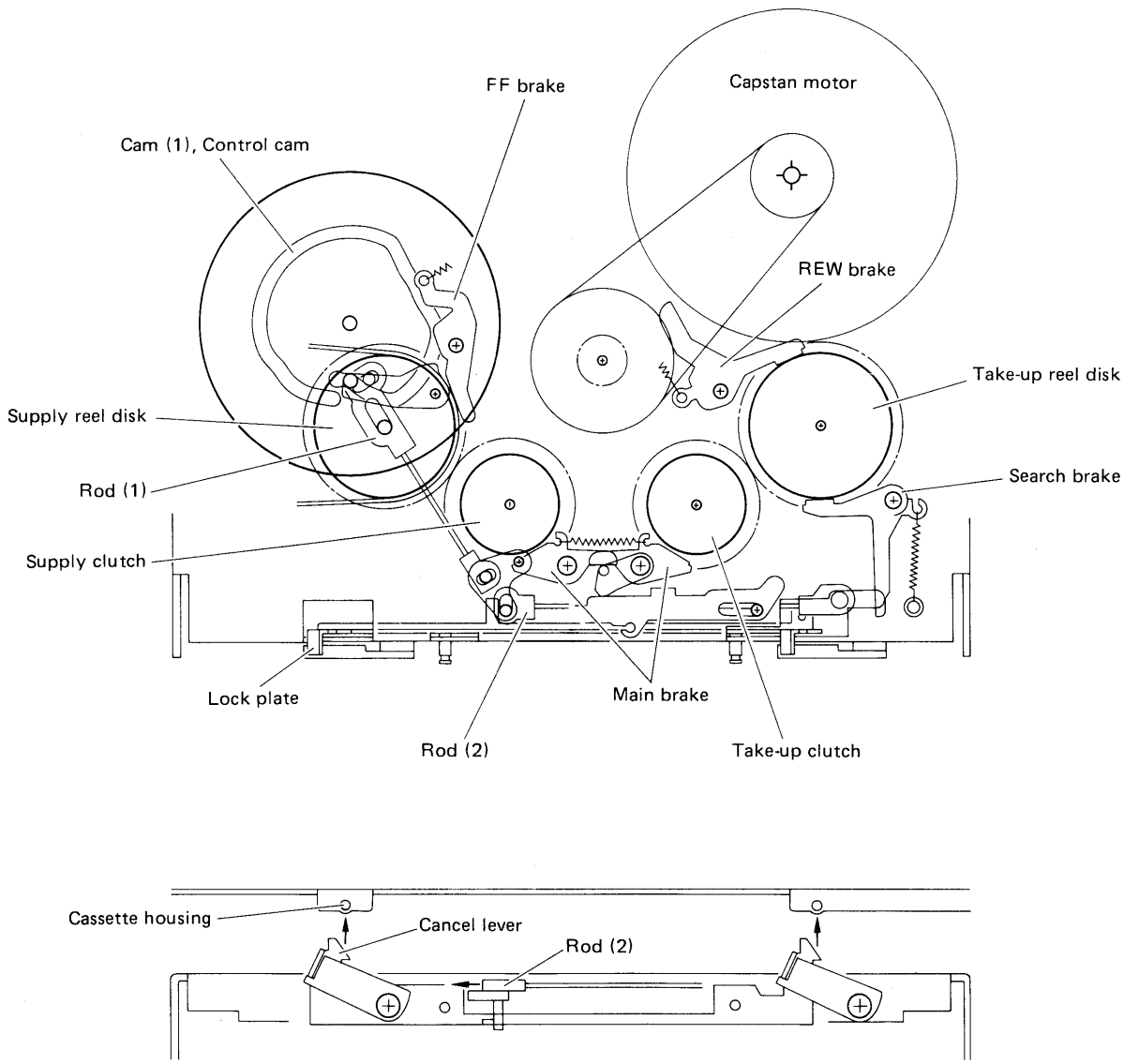
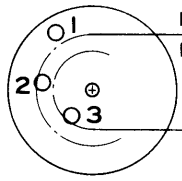


Fig. 6-2-9 Eject mode

6.3 TIMING OF CONTROL CAM



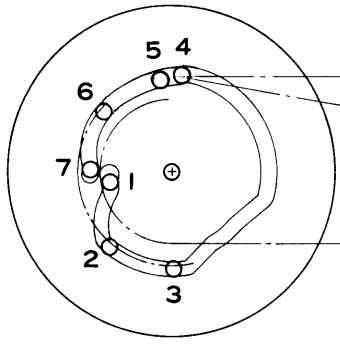
Indicates the mode in which the center is outer side. (No. 1)

Indicates the mode in which the center is inner side. (No. 2, No. 3)

Indicates the mode in which the center is inner side. (No. 3)

Indicates the mode in which the center is outer side. (No. 1, No. 2)

– Cam (1) –



Tension pole lays back-tension on tape. (No. 4 only)

Tension pole is not in operation.

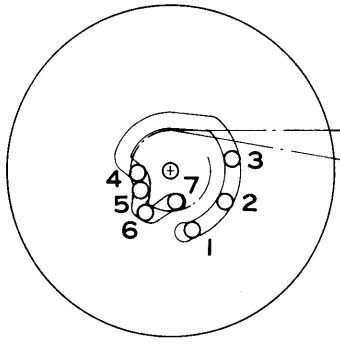
Search brake is off the reel disk.

Search brake contacts the reel disk.

Eject lever is effectual for lock plate.

Eject lever is ineffectual.

– Cam (2) –



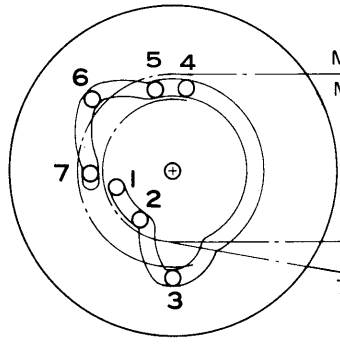
FF (or REW) brake contacts the reel disk.

FF (or REW) brake is off the reel disk.

Pinch roller is off the capstan.

Pinch roller contacts the capstan.

– Cam (3) –



Main brake is in contact with Clutch.

Main brake is off the clutch.

Cam brake is in contact with brake cam.

Cam brake is off the brake cam.

Tape winding by TU idler is possible.

Tape winding by TU gear is possible.

Fig. 6-3-1 Timing of control cam

6.4 A/C HEAD ADJUSTMENT

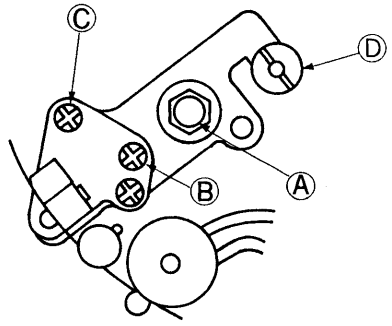


Fig. 6-4-1

● **A/C head**

The A/C head is individually adjustable type.

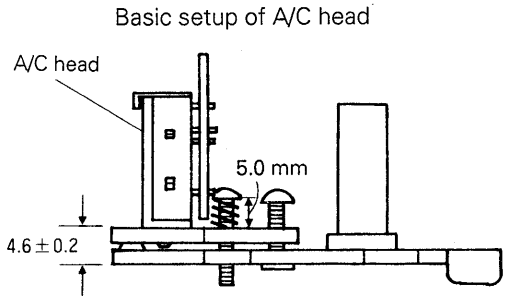


Fig. 6-4-2

Adjusting screw	Adjustment procedure	Illustration
Ⓐ Height adjustment	Adjust the A/C head height to obtain the maximum audio level and the minimum level fluctuation. Use the 7 kHz audio signal of the alignment tape MHP.	Audio waveform
Ⓑ Inclination adjustment	Tilt the A/C head 0.05 to 0.15 mm (horizontal distance between the top and the bottom) in the direction of the tape. Use the parallel check plate (PUJ50204).	A/C head, T.U. guide pole
Ⓒ Azimuth adjustmenmt	Remove phase difference between the audio channel 1 and the audio channel 2. Use the 7 kHz audio signal of the alignment tape MHP.	Remove this phase difference. Audio signal
Ⓓ X-value adjustment	Adjust the phases of the two channels and maximize FM level. Use the alignment tape MBP-X.	Adjust phases of CH-1 and CH-2. 1CH 2CH 1CH 2CH 1CH (FM OUT) AUDIO OUT

Table 6-4-1

6.5 POINTS OF TAPE TRANSPORT ADJUSTMENT

- To turn the guide roller, loosen the setscrew first.
- When the guide roller is turned, perform unloading and loading operation in this order and check FM waveform after that.
- When the taper nut is turned, confirm that both waveforms of the normal audio CH-1 and CH-2 are maximum.
- Before adjusting the height and azimuth of the audio head and the phase of the control head (X-value adjustment), adjust the flange of the Take-up guide pole to accord with the lower edge of the tape.
- Adjust the A/C head perpendicularity to tilt 0.05 to 0.15 mm (center value: 0.1 mm) toward the tape side.
- Make sure to apply screw sealant (to 8 screws).

6.6 APPLYING OF SCREW SEALANT

Apply screw seant (Leichlock ? , No. 3 or equivalent) to the following parts.

- Screw retaining tension band
- Setscrew of the take-up guide arm
- Screws of the A/C head (4 screws)
- Screws of taper nut (2 screws)

6.7 GREASING POINTS

Grease the following parts with Moriton Grease No. 1.

- Control cam
- Lock plate
- Lock pin of the cassette housing
- Drive mechanism of the pinch roller
- Pole base portion

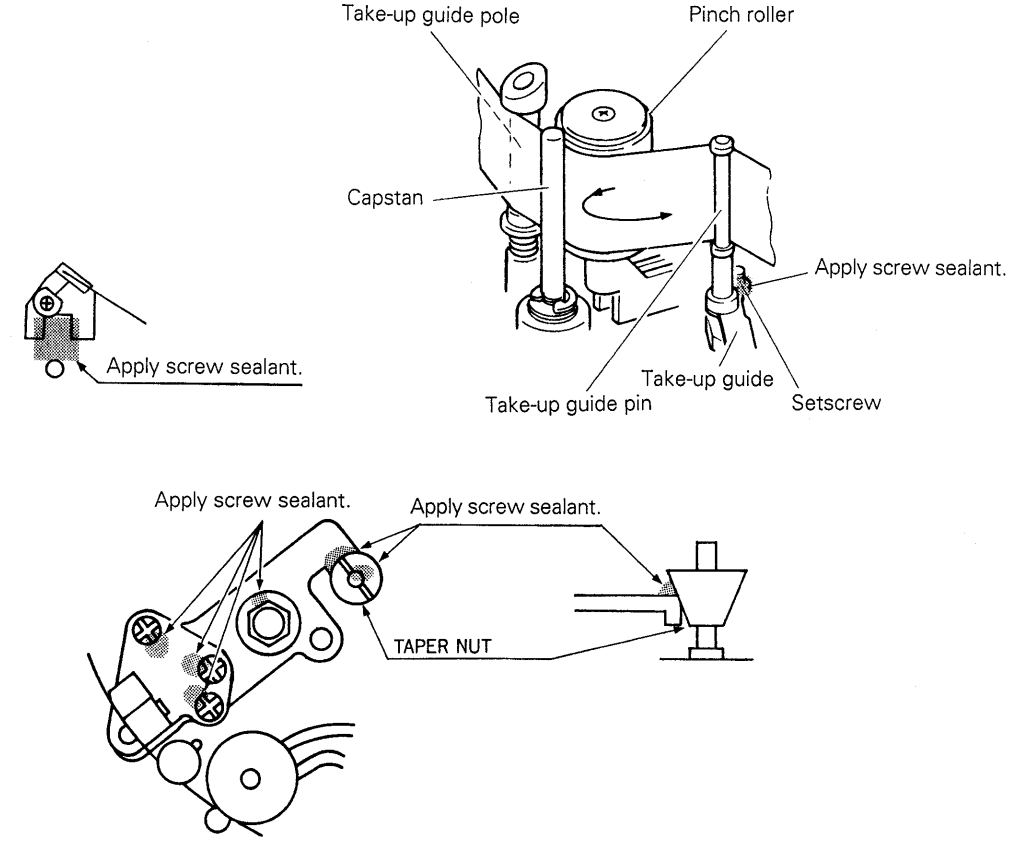


Fig. 6-6-1 Applying of screw sealant

6.8 EMERGENCY EJECT

When the VTR enters the AUTO OFF state and the cassette tape cannot be ejected, take out the cassette tape according to the following procedure.

1. Turn off the power switch of the VTR.
2. Take off the cassette cover so that the tape is exposed. (Remove the screws retaining the cassette cover, and slide the cover upwards while removing it.)
3. Remove the right side cover.
4. Remove the VIDEO board first, and the S/S board.
5. Turn the pulley of the loading motor installed on the back side of the mechanism deck with a screwdriver or the like toward you for unloading the cassette tape gradually. (See Fig. 6-8-1.)
6. If the tape comes loose, turn the pulley of the clutch mechanism to wind the tape for pulling in the slack of the tape.
7. Repeat the above steps 5 and 6 until the tape is restored in the STOP mode. In this condition, slide the lock plate that is locking the cassette housing in the reverse direction of the battery side to eject the cassette tape.

(In the STOP mode, the cassette tape can be ejected by inserting a precision screwdriver through the left side cover and catching the lock plate's pin by it for unlocking. See Fig. 6-8-2.)

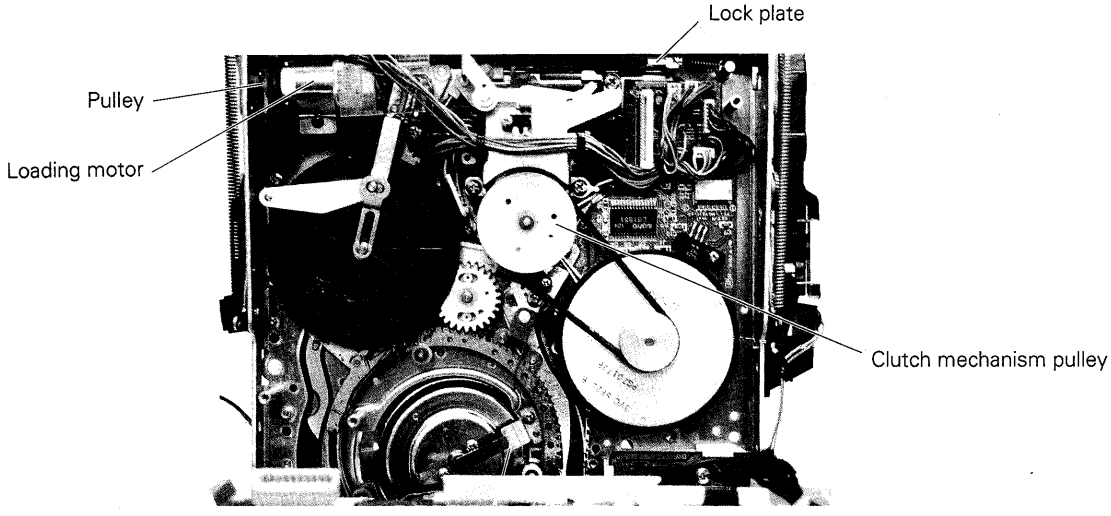


Fig. 6-8-1

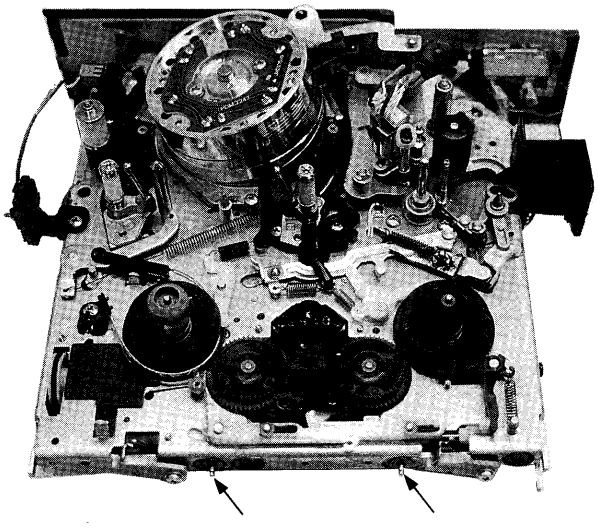


Fig. 6-8-2

SECTION 7
TIME CODE GENERATOR CIRCUIT (SA-R200)

7.1 GENERAL DESCRIPTION

The SA-R200 time code generator which is incorporated in the BR-S422 enables the VTR to write in VITC and LTC time codes comformable to the SMPTE standard.
For recording LTC data the AUD-2 head of the normal audio is used.
When it is intended to record time code in the REC RUN mode, set the AEF switch to the NORMAL position (for zero frame editing) since this VTR is not equipped with any time code reader circuit. When the AEF switch is set to the QUICK position in recording, editing point is overlapped and time code is not continously recorded.
For detail of the time codes, refer to the Video Technical Guide of the BR-S822.

7.2 TIME CODE GENERATOR CIRCUIT

IC1 functions as the time code generator that generates two time code signals of LTC and VITC. LTC output (LTCO) and VITC output (XVTO) are output in the timing as shown in Fig. 7-2-1.
The timing that the syscon presets data to the time code generator is shown in Fig. 7-2-2.

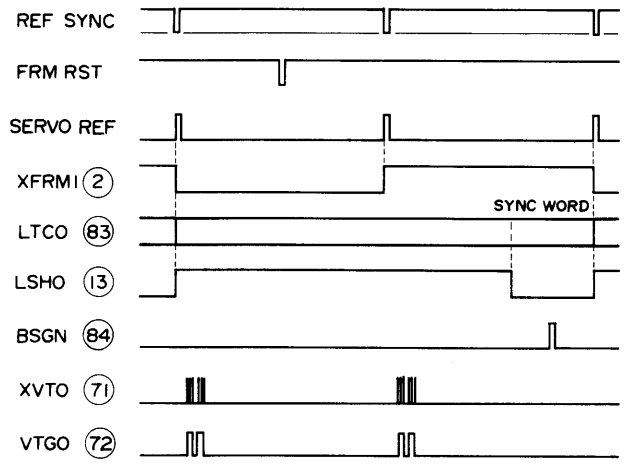


Fig. 7-2-1 Time code generator timing chart

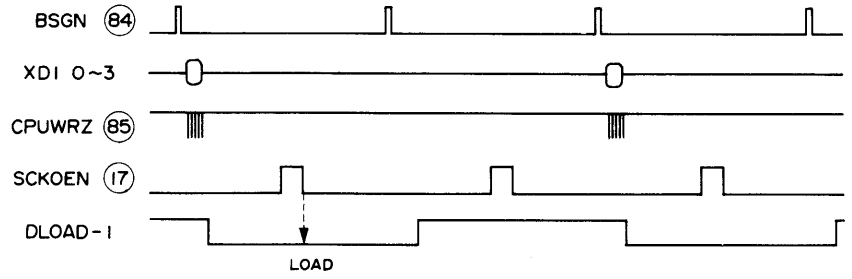
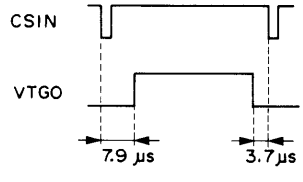


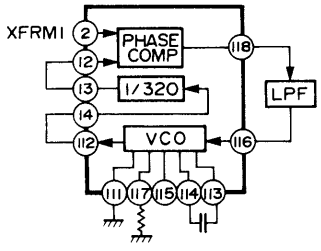
Fig. 7-2-2 Data preset timing

Pin No.	Pin Name	I/O	Description
1, 26, 47, 70, 90, 107	GND	I	GND
2	XFRMI	I	Frame signal input
6 7	VDI VDO	I O	V. sync drive input ← V. sync drive output ← VD signal separated from CSIN signal of pin ⑩
8 9	HDI HDO	I O	H. sync drive input ← H. sync drive output ← HD signal separated from CSIN signal of pin ⑩
10	CSIN	I	Composite sync signal input
12 13	LSHI LSHO	I O	LTC synchronous signal "H" input ← LTC synchronous signal "H" output ← To synchronize start bit of LTC output with video signal.
14	LCKI	I	LTC clock input - To generate LTC sync signal (×1 speed : 9.6 kHz)
19 20 21	LSBO LSCO LSDO	O O O	LTC sync signal B output LTC sync signal C output LTC sync signal D output Synchronizing with output LTC. External multiplexer is controlled with these signals to input serial signal to input port of pin ㉒ – ㉕ .
22 23 24 25	PORT A PORT B PORT C PORT D	I I I I	Serial signal input ports
27 28 29	IS1 IS2 IS4	I I I	INPUT SIGNAL FORMAT SELECT 1 INPUT SIGNAL FORMAT SELECT 2 INPUT SIGNAL FORMAT SELECT 4

DF/NDF SW	S1	S2	S4	Signal Name	System
DF	H	H	H	NTSC DROP FRAME	525/60
NDF	L	H	H	NTSC NON-DROP FRAME	525/60
—	L	L	H	PAL/SECAM	625/50
—	L	L	L	FILM	655/48

30	PCLR	I	Power ON clear input ⎍
49	LTCI	I	LTC input Time code input only in normal bit rate (×1 speed)
63	BSCT	O	BUSY CTL signal output H : During control data output just after CTL pulse fall
64	CTLI	I	CTL signal input CTL counter is stepped up at this trailing edge.
65	FWRE	I	CTL direction signal input FWD|REV To input signal indicating tape transport direction at stepup by CTLI signal
66	CTLRST	I	CTL reset signal input
67	DLOD3	I	DATA LOAD 3 input Signal input to load control data with XDI0–3
68	CTCT	I	CTL counter mode select input H : 24H mode, L : 10H mode
69	CTLDI	I	CTL DISENABLE - Input signal to inactivate pin ⑥③ BSCT H : BSCT inactivated (CTL data is output when pin ⑧④ BSGN is "H".)
71	XVTO	O	VITC output
72	VTGO	O	VITC gate signal output H : VITC insertion line



Pin No.	Pin Name	I/O	Description
82	LTCPHASE	I	LTC phase select input
83	LTCO	O	LTC output
84	BSGN	O	BUSY GENERATOR Output in and around center of LTC SYNC WORD. Data access inhibited during this output
85	CPUWRZ	I	CPU write signal input Signal input to get CPU to load data directly to XDI1–3
86 87 88 89	XDI3 (MSB) XDI2 XDI1 XDI0 (LSB)	I I I I	Data input Signal input for direct loading of 4 bits hexadecimal data such as time data, user's bit data, CTL data
91 92 93 94 95 96	AD0 AD1 AD2 AD3 AD4 AD5	I/O I/O I/O I/O I/O I/O	Address data input/output · Address signal output to indicate output data · Address signal input for data access to internal RAM and MPX.
97	XACS	I	Address line output enable H : Address output terminals are OFF (high impedance)
98 99 100 101	XDO0 (LSB) XDO1 XDO2 XDO3 (MSB)	O O O O	Data output (4 bits hexadecimal data) Generation data or CTL data is output depending on mode.
102	XDCS	I	Data line output enable H : Data output terminals XDO0–3 getting high impedance
104	CPURDZ	I	CPU read signal input Signal input to enable CPU to strobe output signal of XDO0–3
105	CLK7MO	O	7 MHz clock output (Inversion output of clock that pin (109) CKIN signal is half divided)
106	SLCK	I	Select clock input To select CKIN frequency. L : 14.318 MHz, H : 7.159 MHz
108	XCKO	O	Clock output (Inversion output of pin (109) CKIN signal)
109	CKIN	I	System clock input (14.318 MHz)
111 112 113 114 115 116 117 118	INH1 VCOOUT CIB CIA R2 VCOIN R1 PHCOUT	 O I I I I I O	

	TC	UB	RT	CTL
AD3	L	H	H	H
AD4	L	L	H	L
AD5	L	L	L	H

Table 7-2-1 IC1 time code generator (VC2067A) pin functions

• **Serial input signal**

Each port of pins 22 to 25 of IC1 time code generator is supplied with 8-bit serial signals which the multiplexers IC8 to IC11 generate by converting parallel signasl into serial signals (Fig. 7-2-3). At that time, the multiplexers are controlled by LSBO, LSCO and LSDO outputs from pins 19 to 21 of IC1.

Four kinds of serial signals generated by the above process are shown in Table 7-2-2.

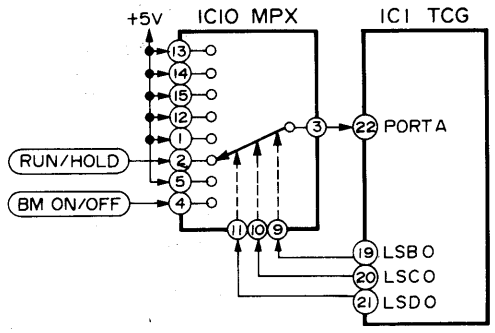


Fig. 7-2-3 Parallel-serial converter circuit

Pin No.	Signal Name		Description							
			0	1	2	3	4	5	6	7
18	SCK O									
19	LSB O									
				←0.4ms→						
20	LSC O									
21	LSD O									
22	PORT A		TC/UB	UB/RT	TCUB/CTL	RT	UB	RESET	RUN/HOLD	BM
		H	TC	UB	TC·UB	OFF	VITC	OFF	RUN	OFF (DIP SW 3-1)
		L	UB	REAL TIME	CTL	ON	LTC	ON	HOLD	ON
23	PORT B		SLAVE	SSEL 0	SSEL 1	SLEB	ERCLR	DLOD 1	DLOD2	VITC
		H	OFF	RESET	RESET	2	OFF	DATA LOAD	DATA LOAD	E1 (JP1)
		L	ON	SET	SET	8	ON	(TC)	(UB)	E2
24	PORT C		AS 1	AS 2	AS 3	AS4	AS 5	AS6	AS 7	AS 8
		H	RESET (DF)	RESET (CF)	RESET (BM)	RESET	RESET (SW8-2)	RESET	4FIELD	FIELD1 INPUT
		L	SET	SET	SET	SET	SET	SET	8FIELD	
25	PORT D		SW1A	SW2A	SW3A	SW4A	SW1B	SW2B	SW2C	SW2D

SW1A/SW1B	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
SW2A/SW2B	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
SW3A/SW3B	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
SW4A/SW4B	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
VITC INSERTTON LINE No.	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10

Note 1: In the above table, indications in the box are always fixed in those conditions.

Note 2: Port C controls on/off of assinged bits. AS1 to AS6 are assigned to the following bits.

	LTC	VITC	Remark
AS1	10	14	Drop Frame Flag
AS2	11	15	Color Frame Flag
AS3	27	35	LTC Bi-phase Mark Phase Correction Bit or VITC Field Mark Bit (Settable by DIP switch SW3-1 on the DISPLAY board)
AS4	43	55	Binary Group Flag Bit
AS5	58	74	Unassigned Address Bit
AS6	59	75	Binary Group Flag Bit

Table 7-2-2 Parallel-serial signal conversion

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